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CAD Note:
Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place
S or DB = Replace after Debug

Schematics Change History

[illegible]

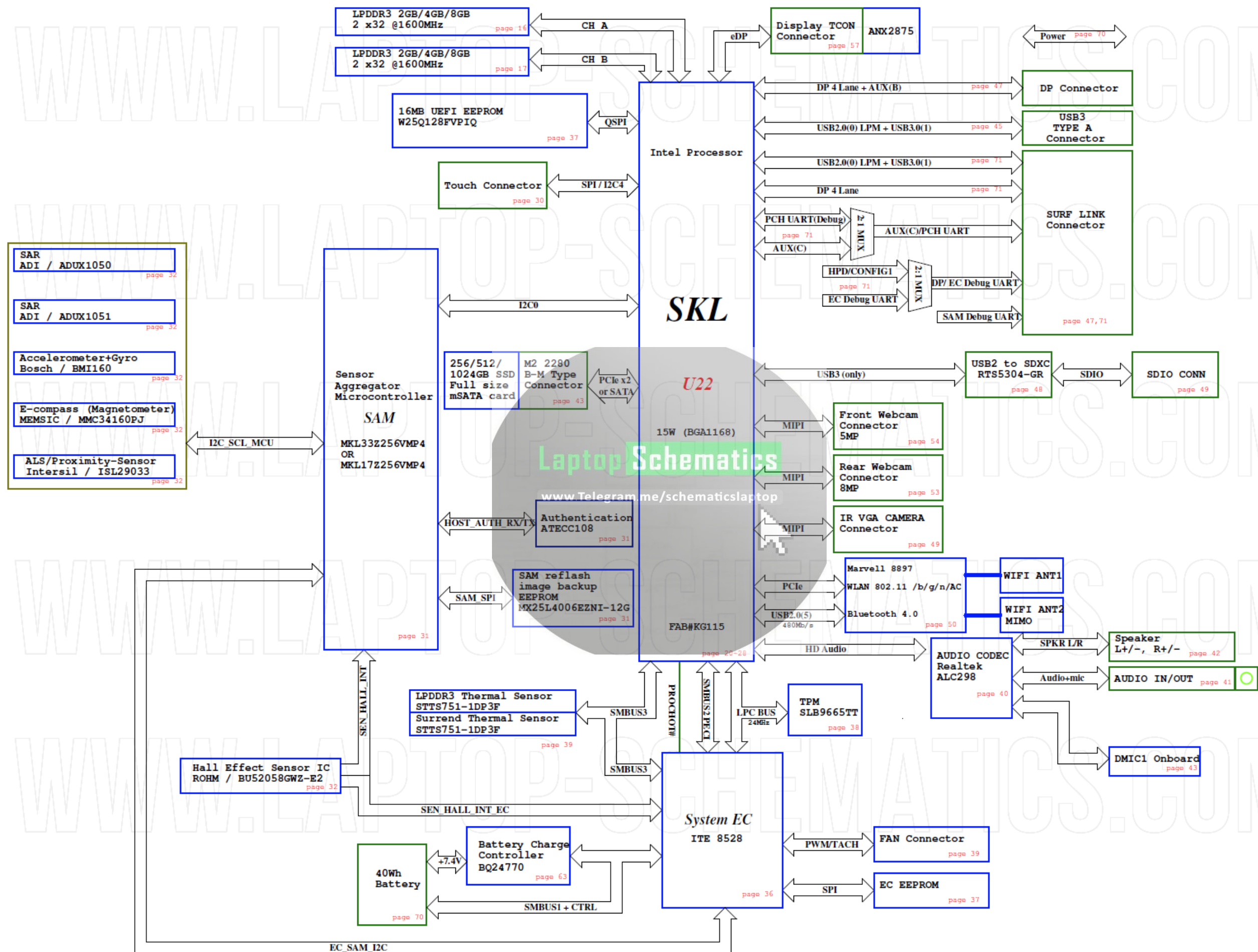
CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

Property: BUILD-OPT

DNP = Not Installed Part.



DIMM2

DIMM1

M_CHA_CLK[0..1]/#
M_CHB_CLK[0..1]/#

Intel
SKL U/Y

SUS_CLK

WIFI_32K_CLK
32 KHz

88W8897-XX-CBK2

CLKOUT_LPC_0

CK_24M_EC
24 MHz

ITE 8528VG/FX

32.768KHz

CK_24M_DEBUG
24 MHz

LPC DEBUG HEADER

CLKOUT_LPC_1

CK_24M_TPM
24 MHz

TPM

CLKOUT_ITXDP_N
CLKOUT_ITXDP_P

CLK_XDP_N
CLK_XDP_P
100 MHz

XDP

CLKOUT_PCIE_N2
CLKOUT_PCIE_P2

PCIE_WIFI_RCLK_N
PCIE_WIFI_RCLK_P
100 MHz

WIFI

CLKOUT_PCIE_N4
CLKOUT_PCIE_P4

PCIECLK_SL1_N
PCIECLK_SL1_P
100 MHz

SLI

HDA_BCLK

AZ_BITCLK
24 MHz

AUDIO CODEC

SPI_CLK

SPI_CLK
50 MHz

SPI ROM

XTAL24_IN

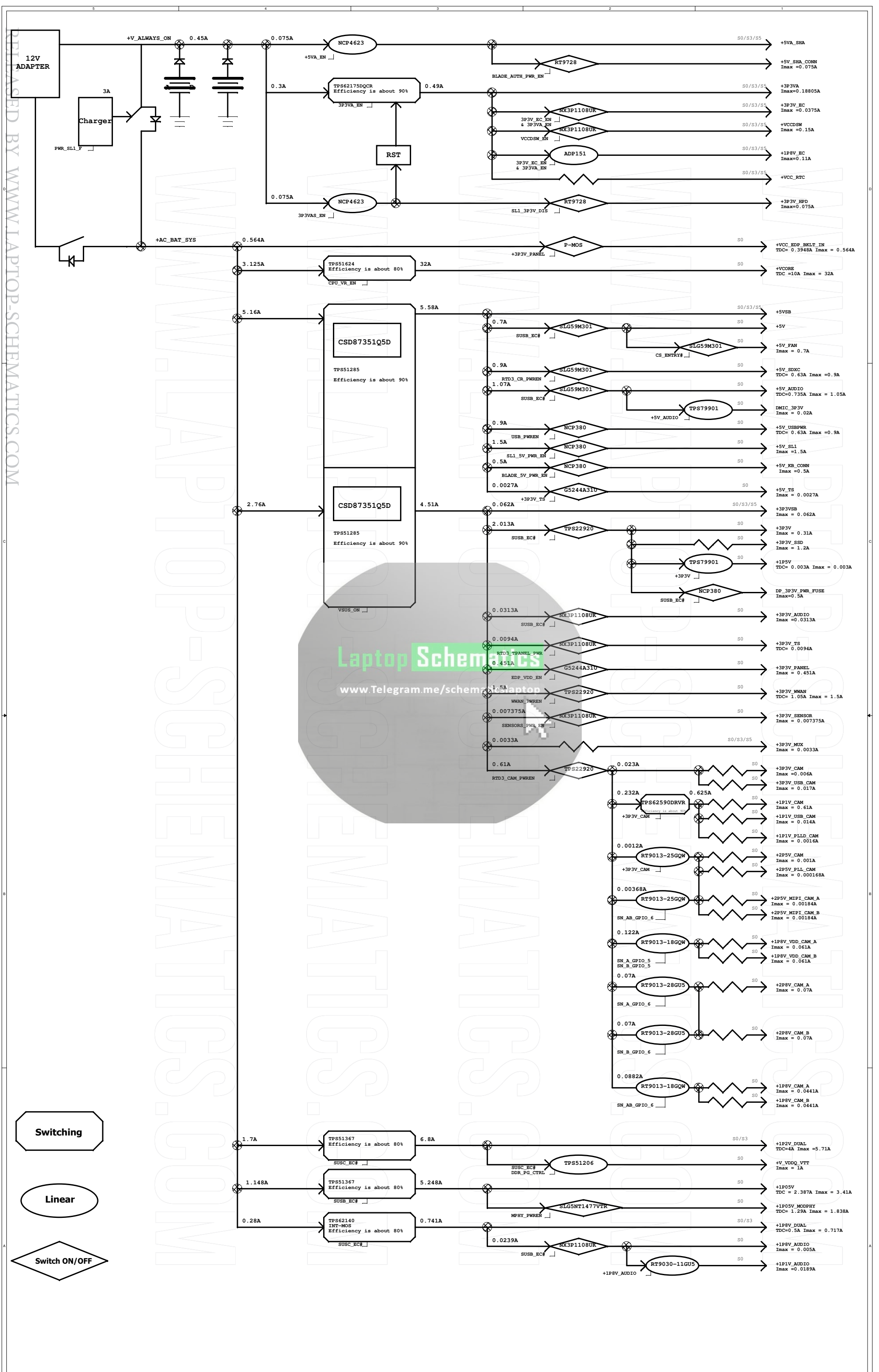
RTCX

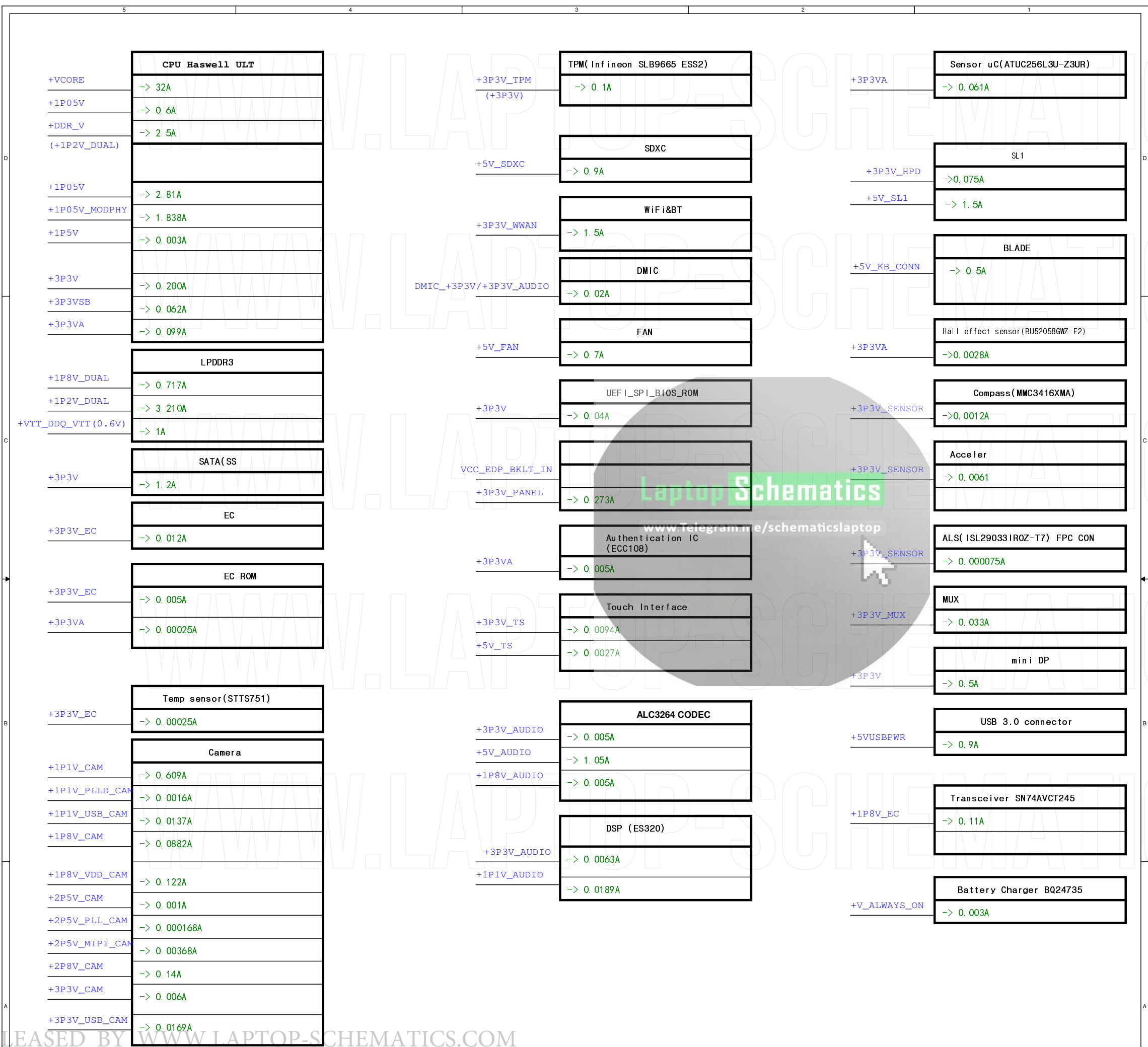


24MHz

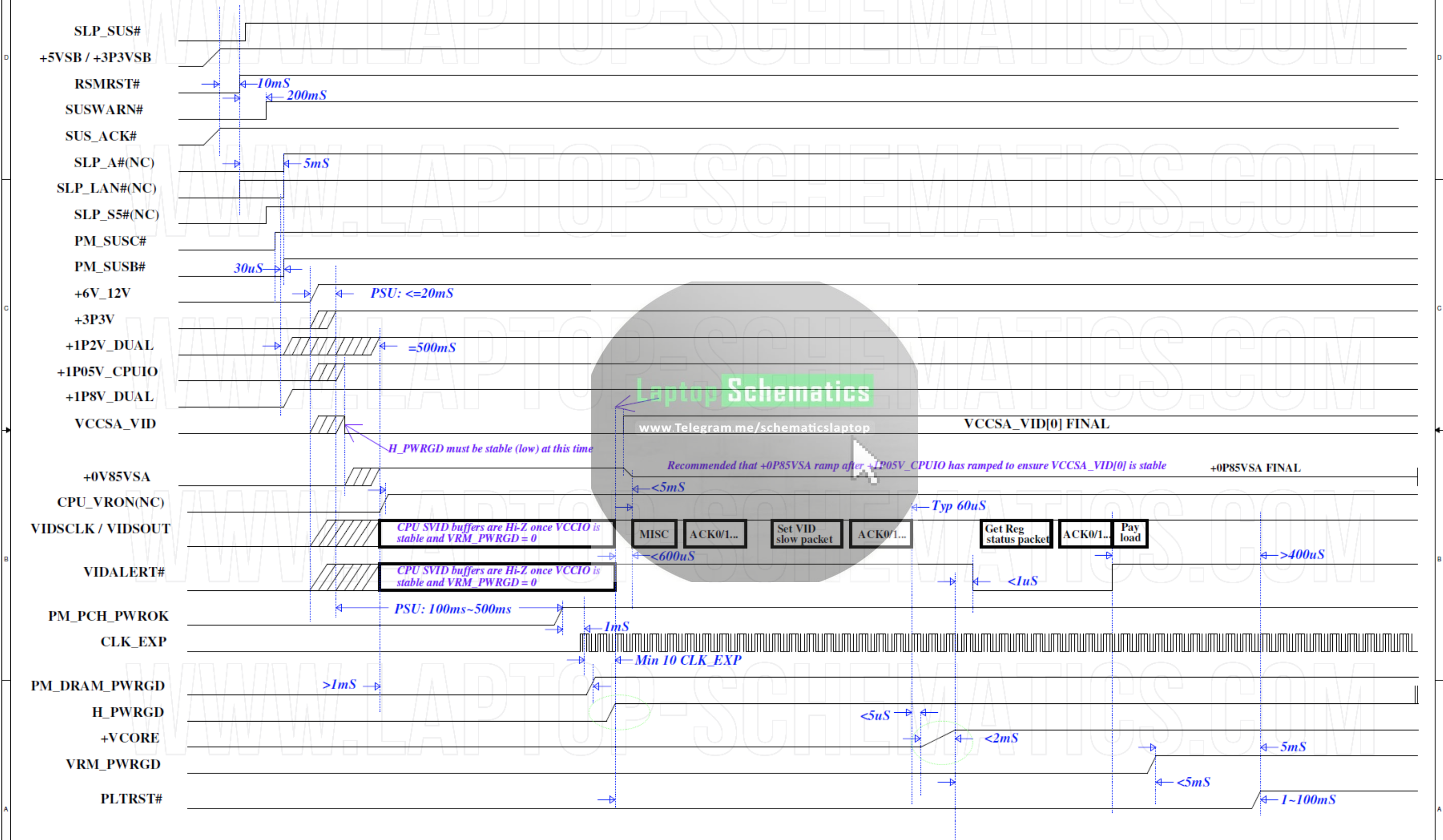


32.768KHz

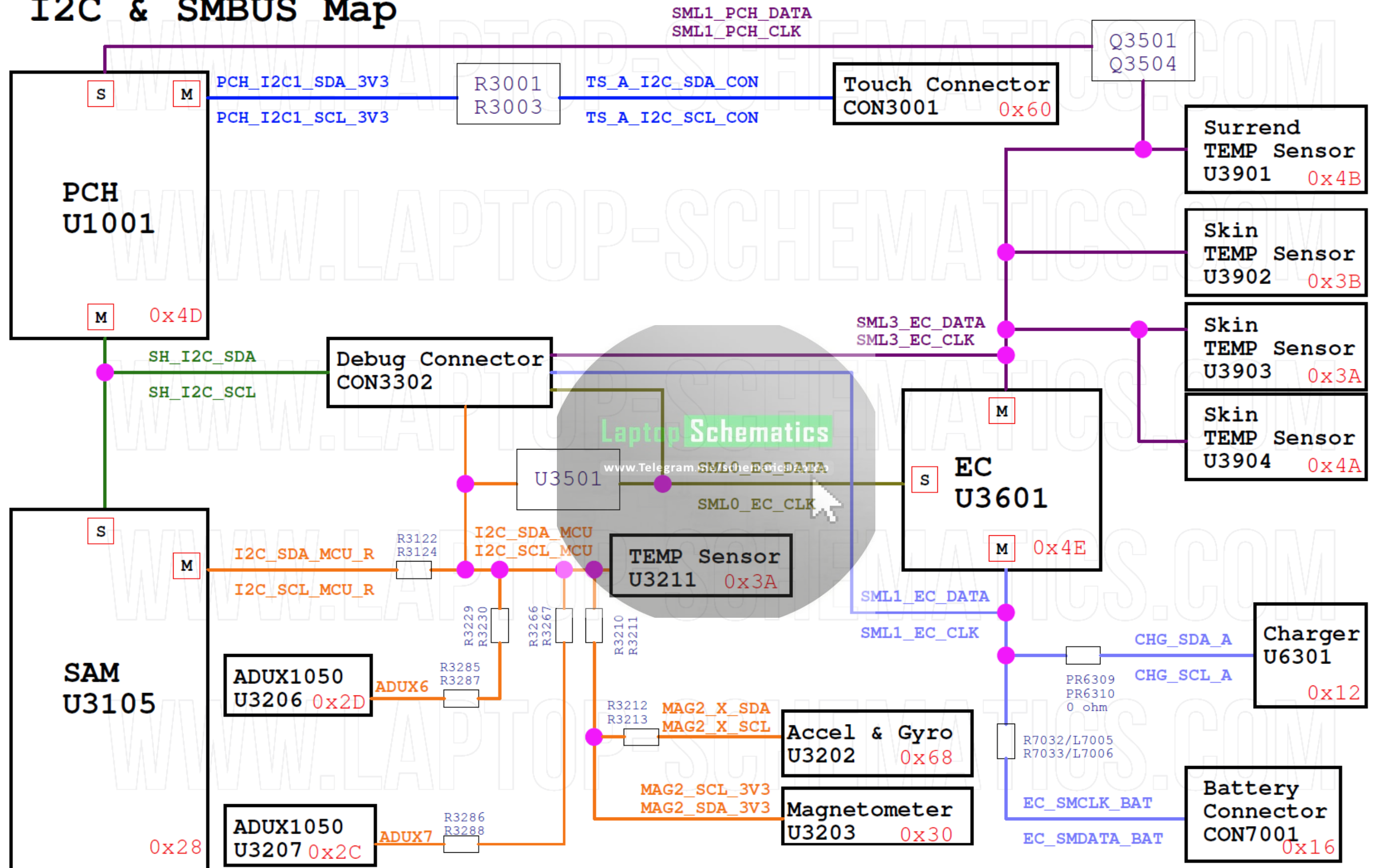


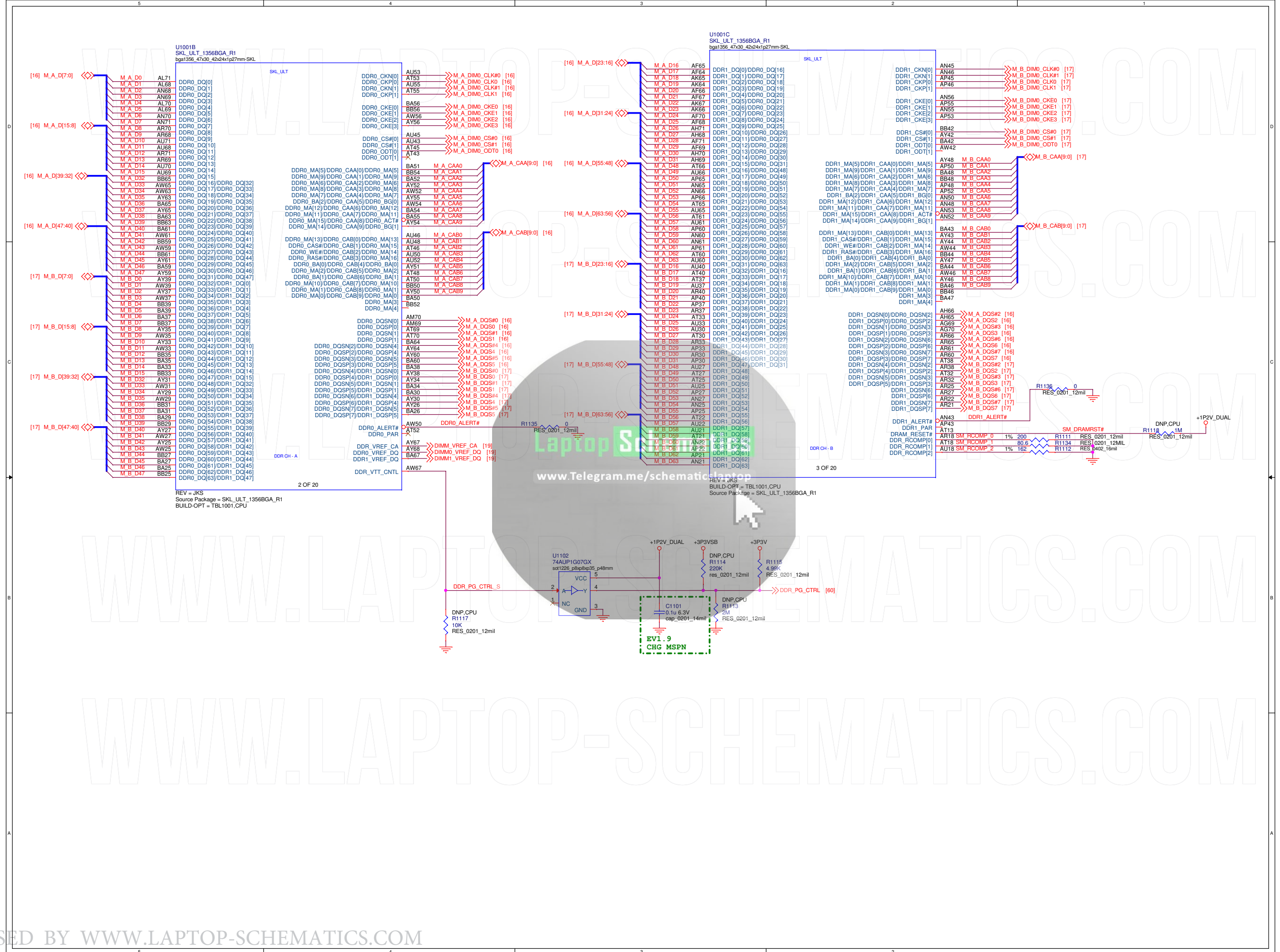


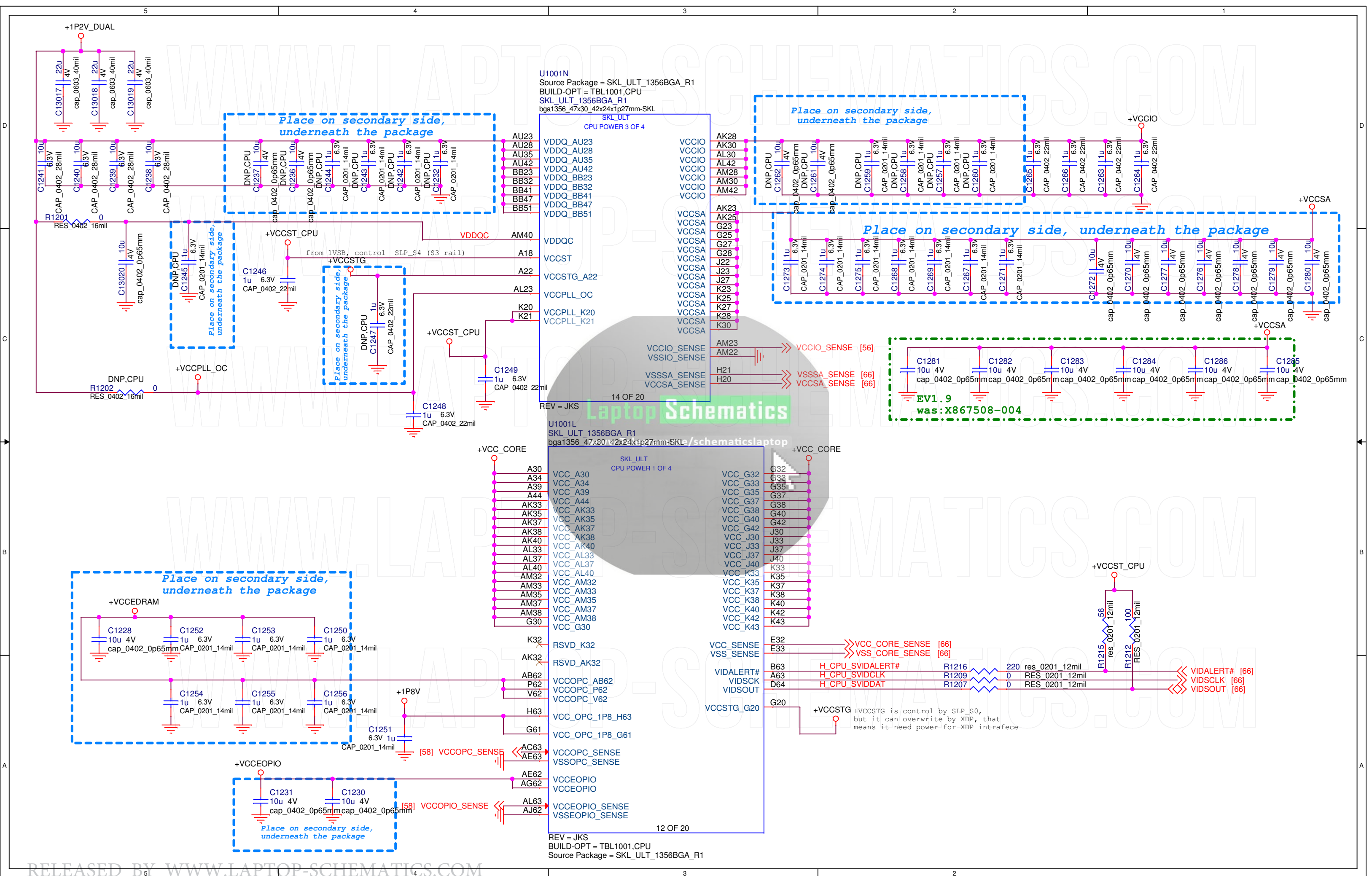
S5 to S0 Power Sequence

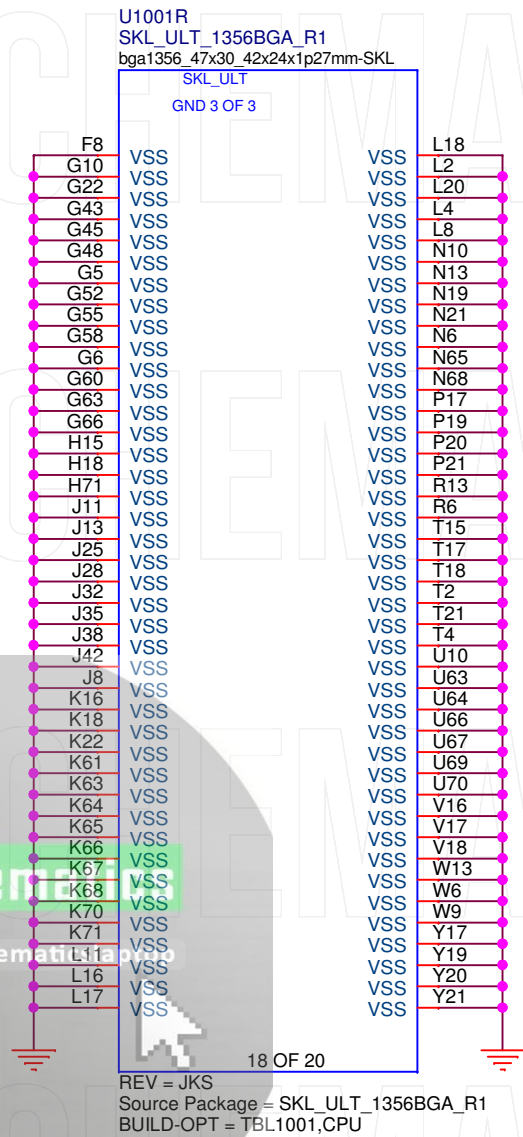
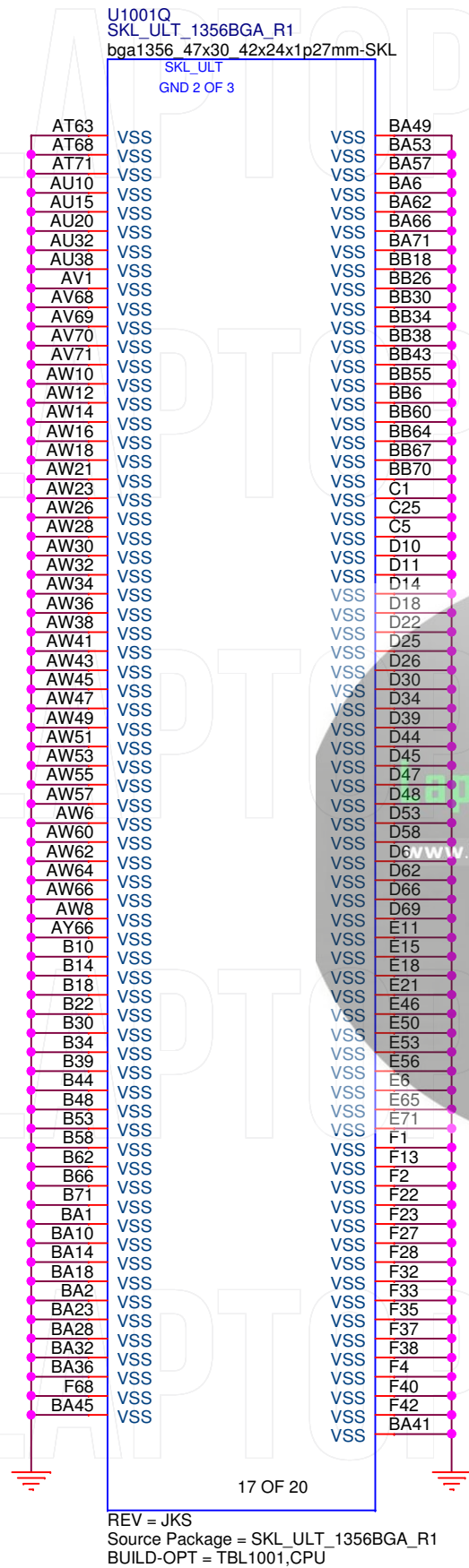
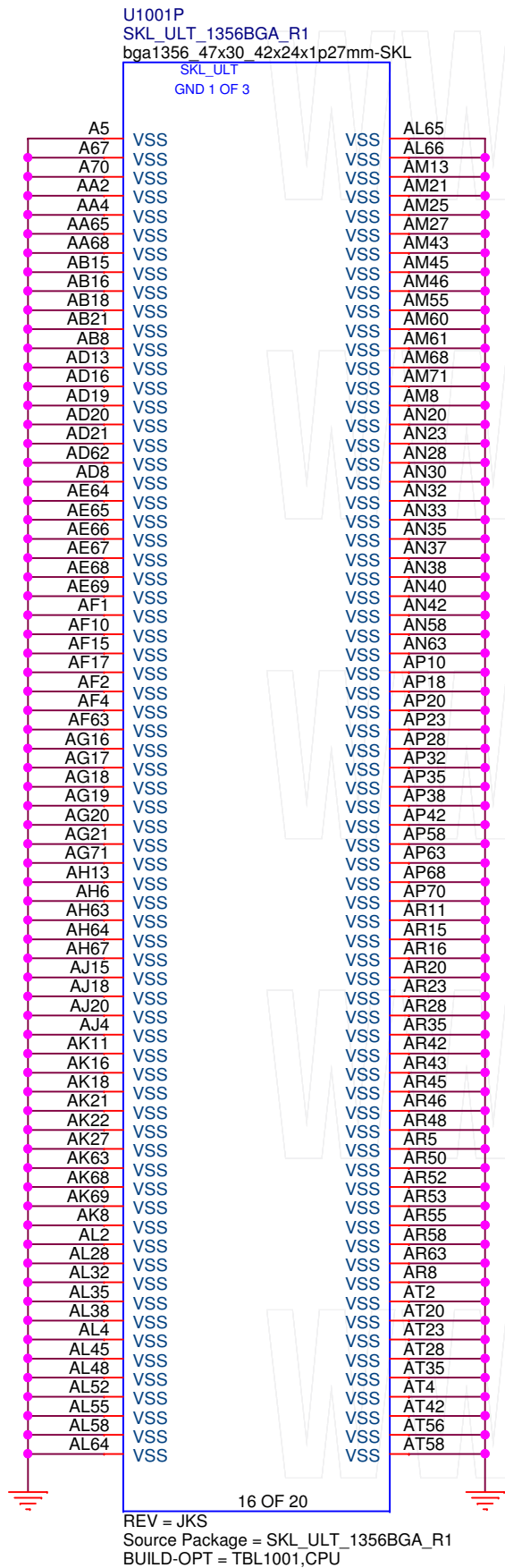


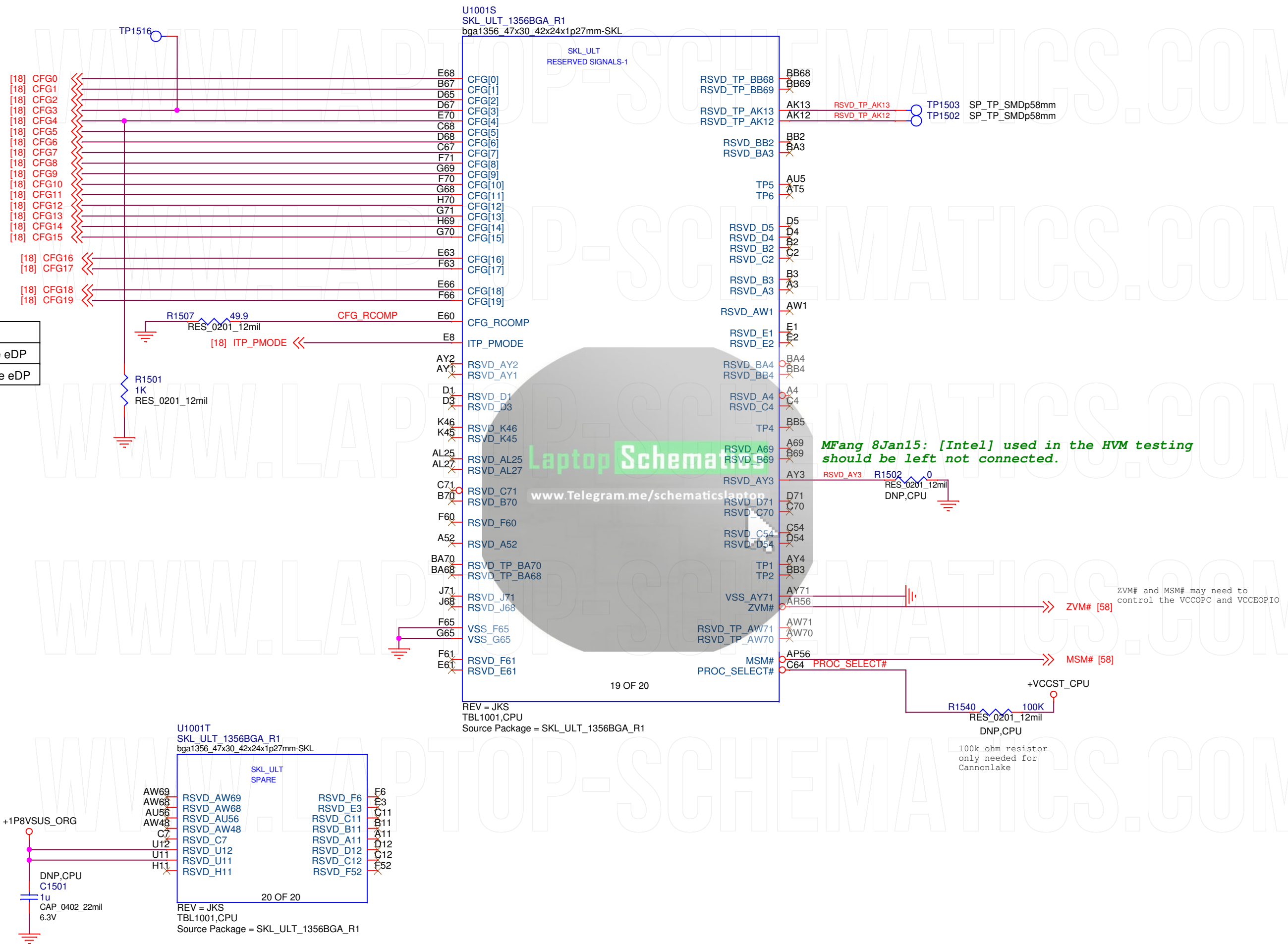
I2C & SMBUS Map

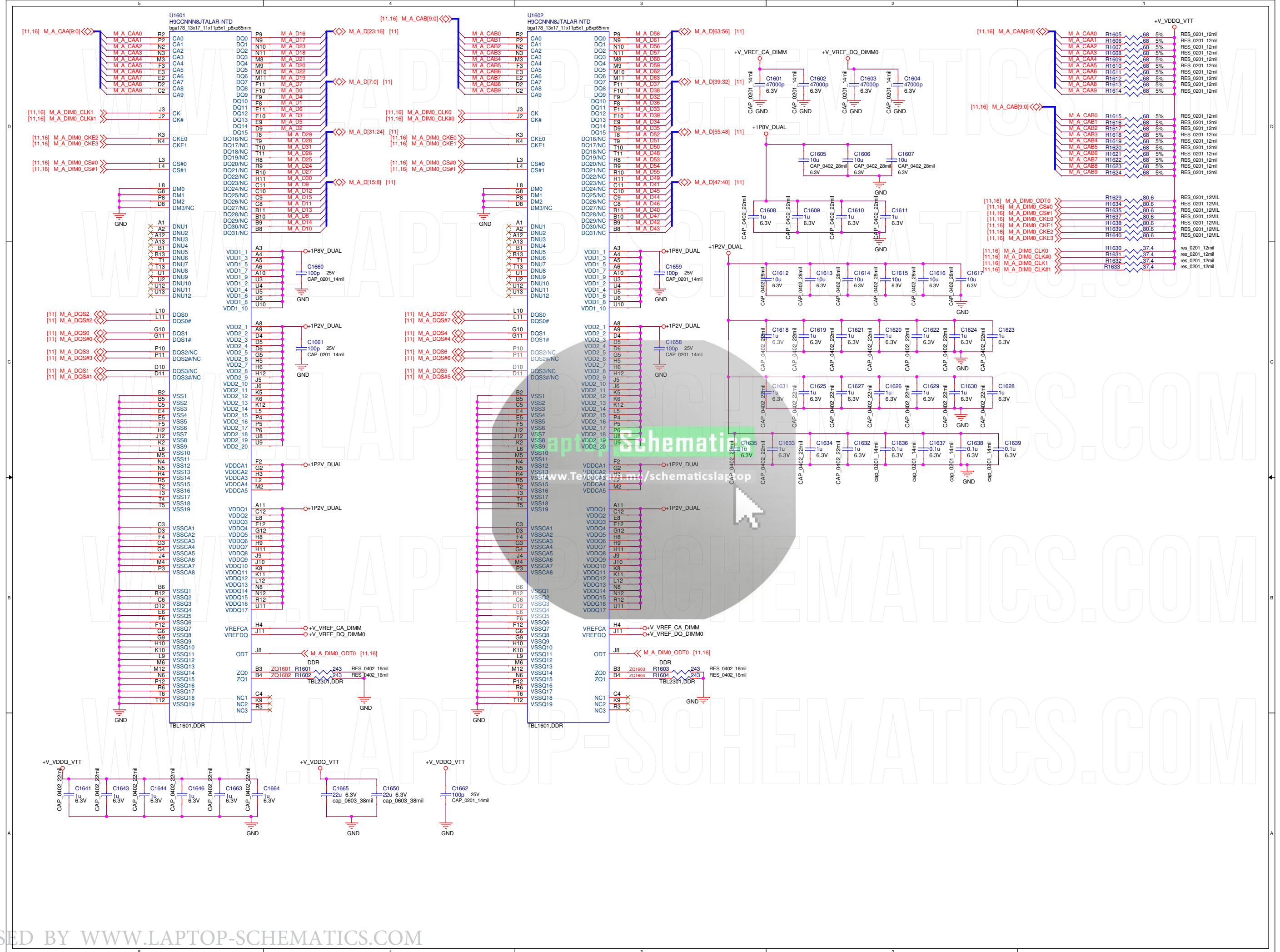


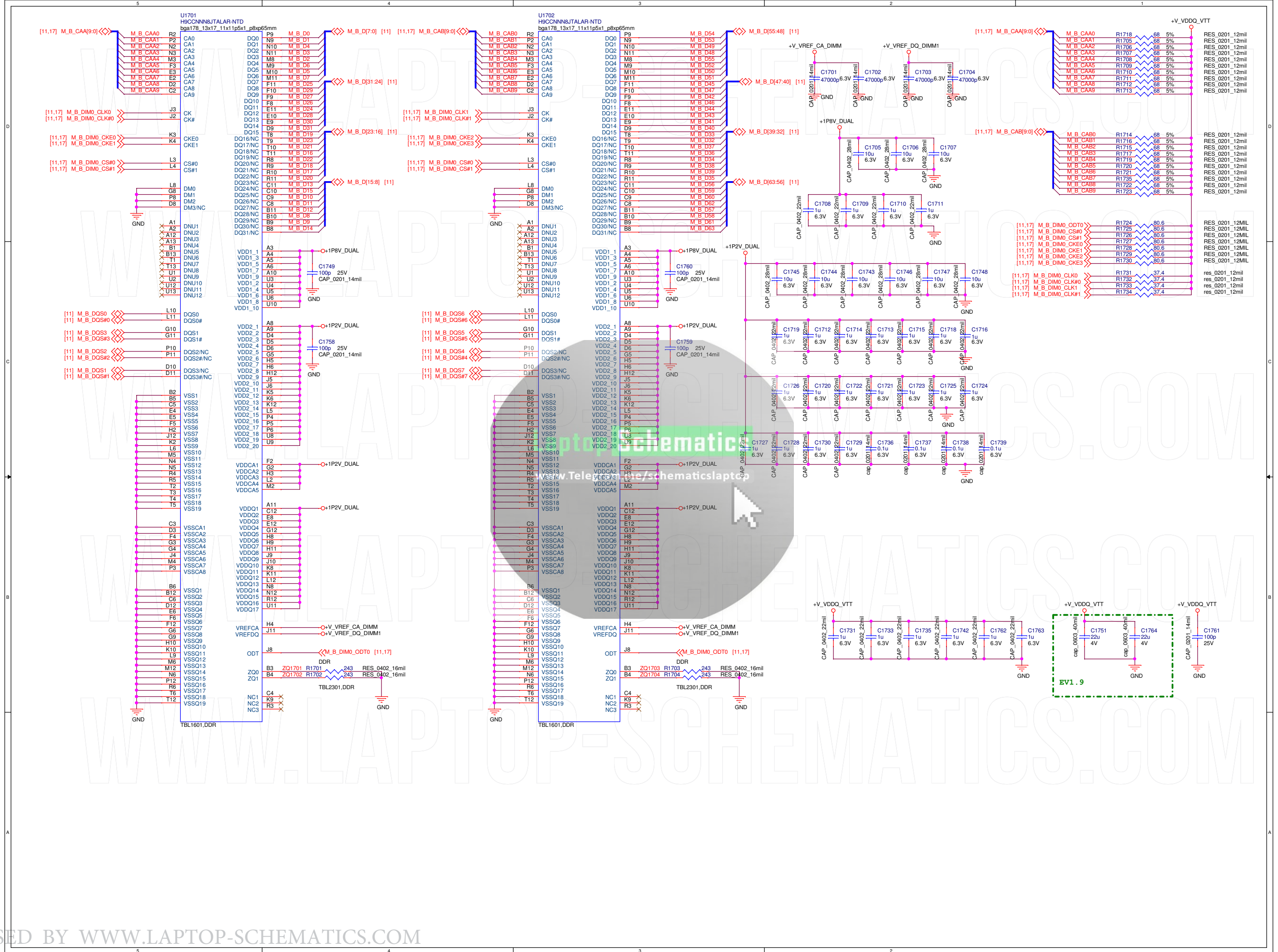






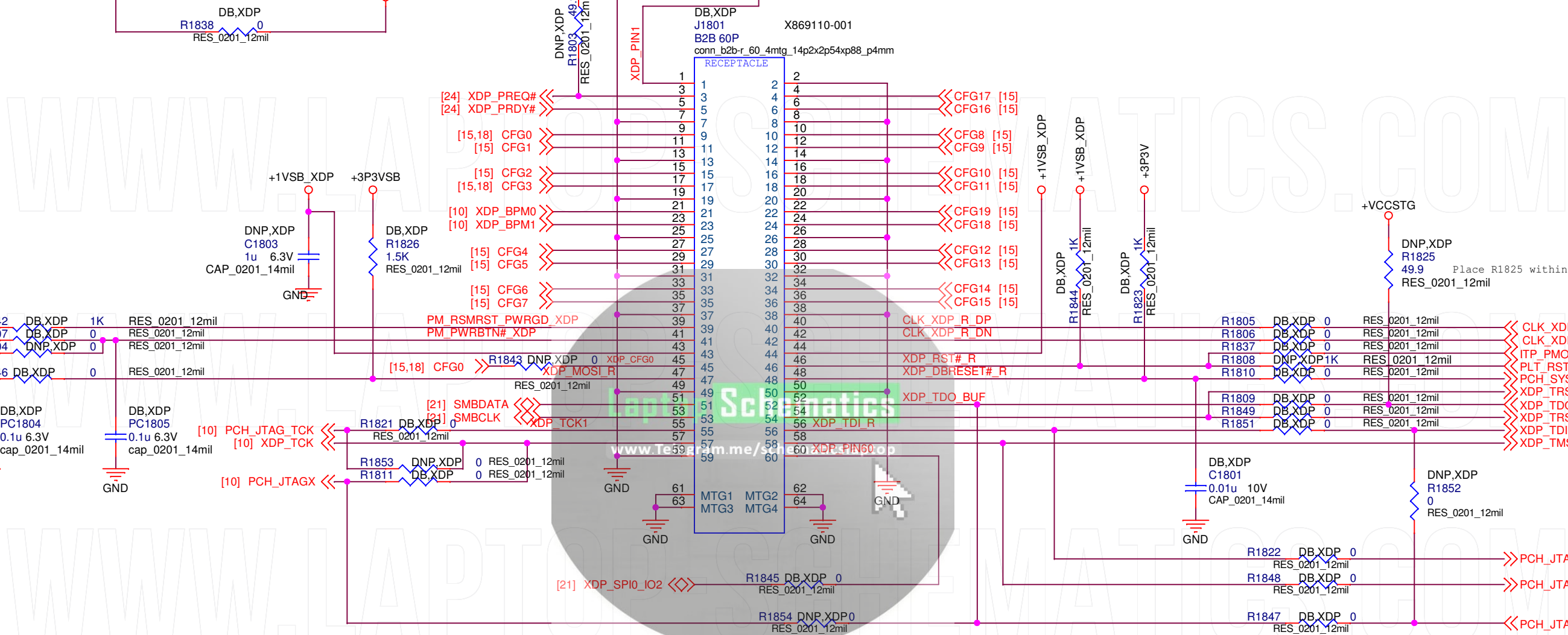






The schematic diagram for the PRIMARY XDP connector shows the following components and connections:

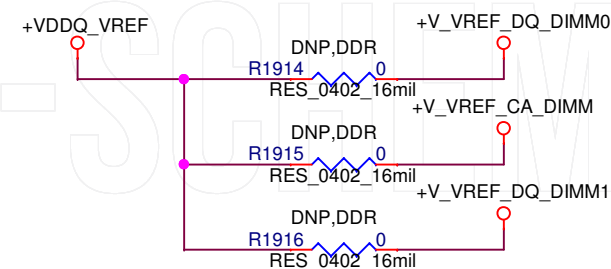
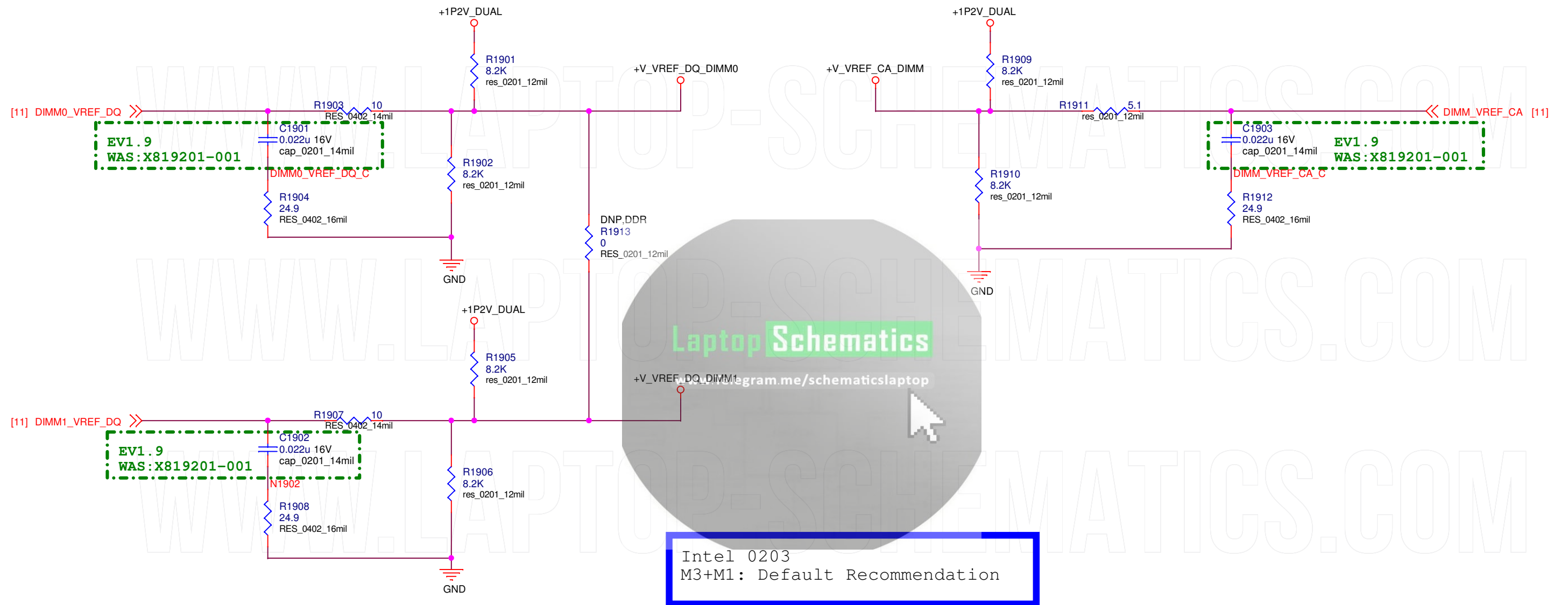
- Power Inputs:**
 - +1VSB:** Connected to the left side of the DB,XDP connector.
 - +1VSB_XDP:** Connected to the left side of the DB,XDP connector.
- DB,XDP Connector:**
 - Pin 1:** Labeled **DB,XDP R1841 1K RES_0201_12mil**.
 - Pin 2:** Labeled **DB,XDP RES_0201_12mil R1840 0**.
- Configuration:**
 - [15,18] CFG3** is indicated with a red arrow pointing to the DB,XDP connector.
 - A note states: **ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG3<3>**.

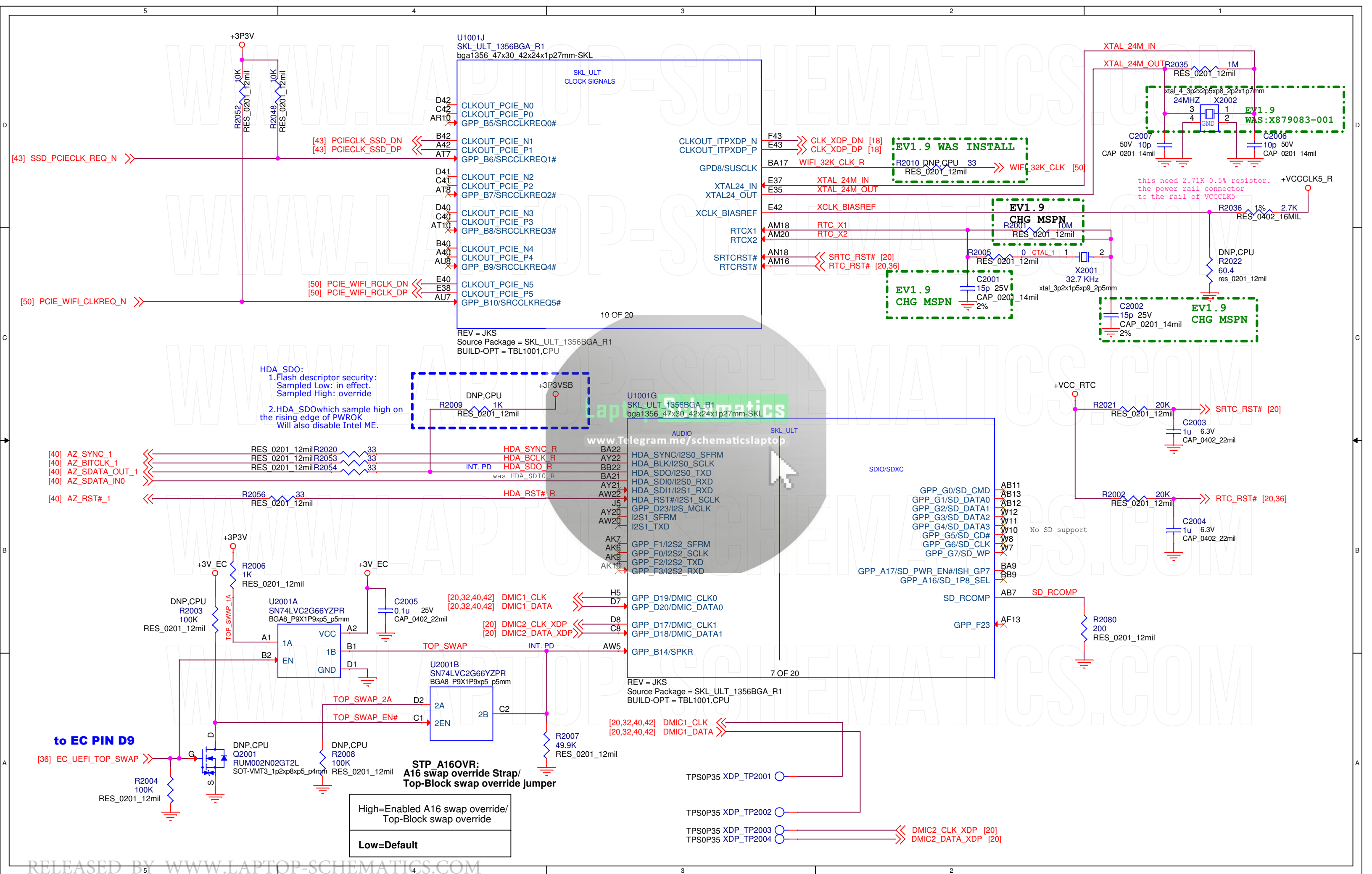


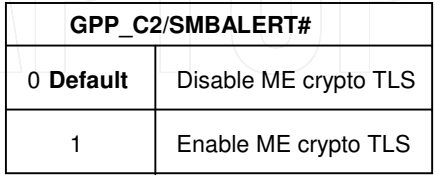
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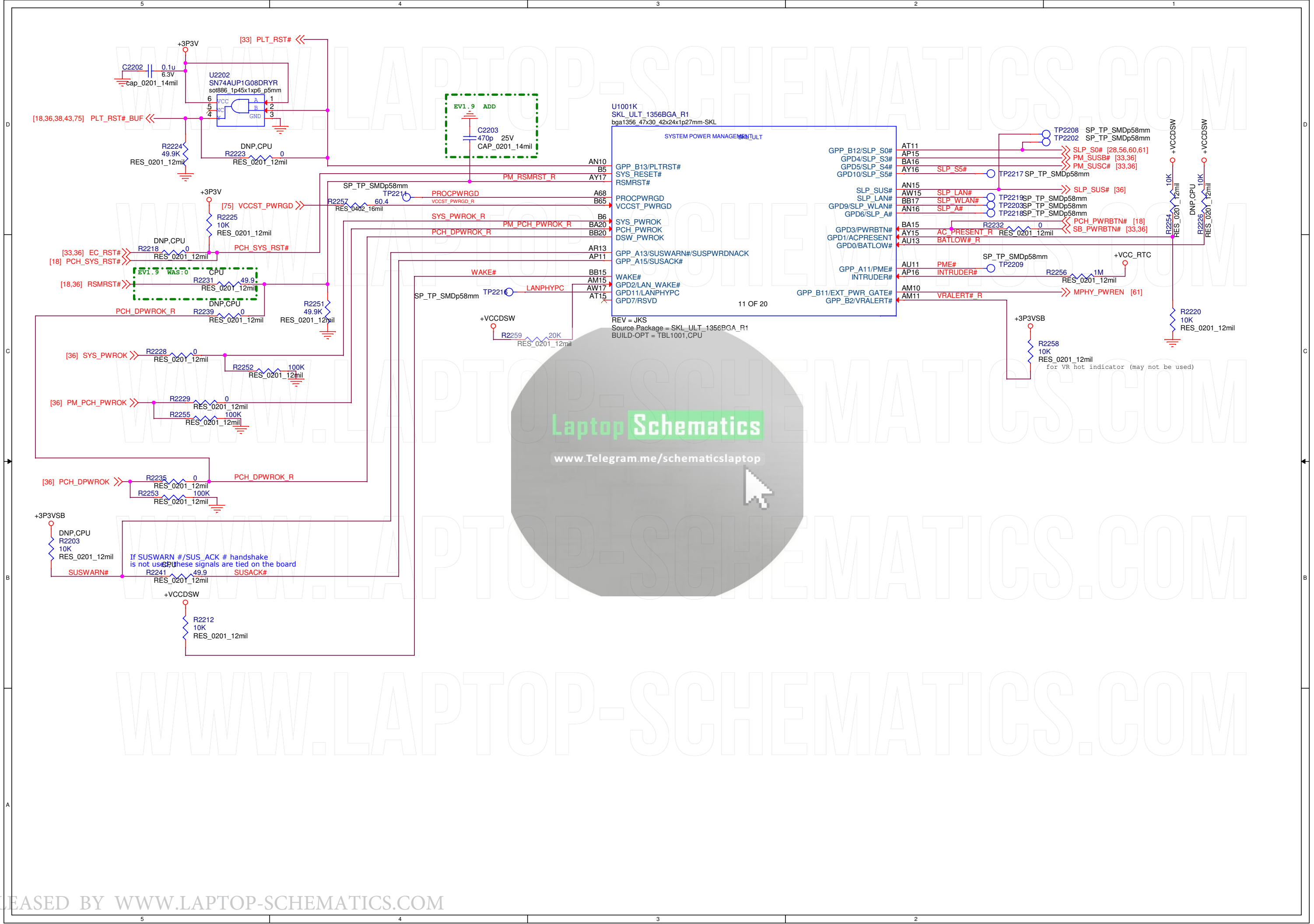
LPDDR3 Vref

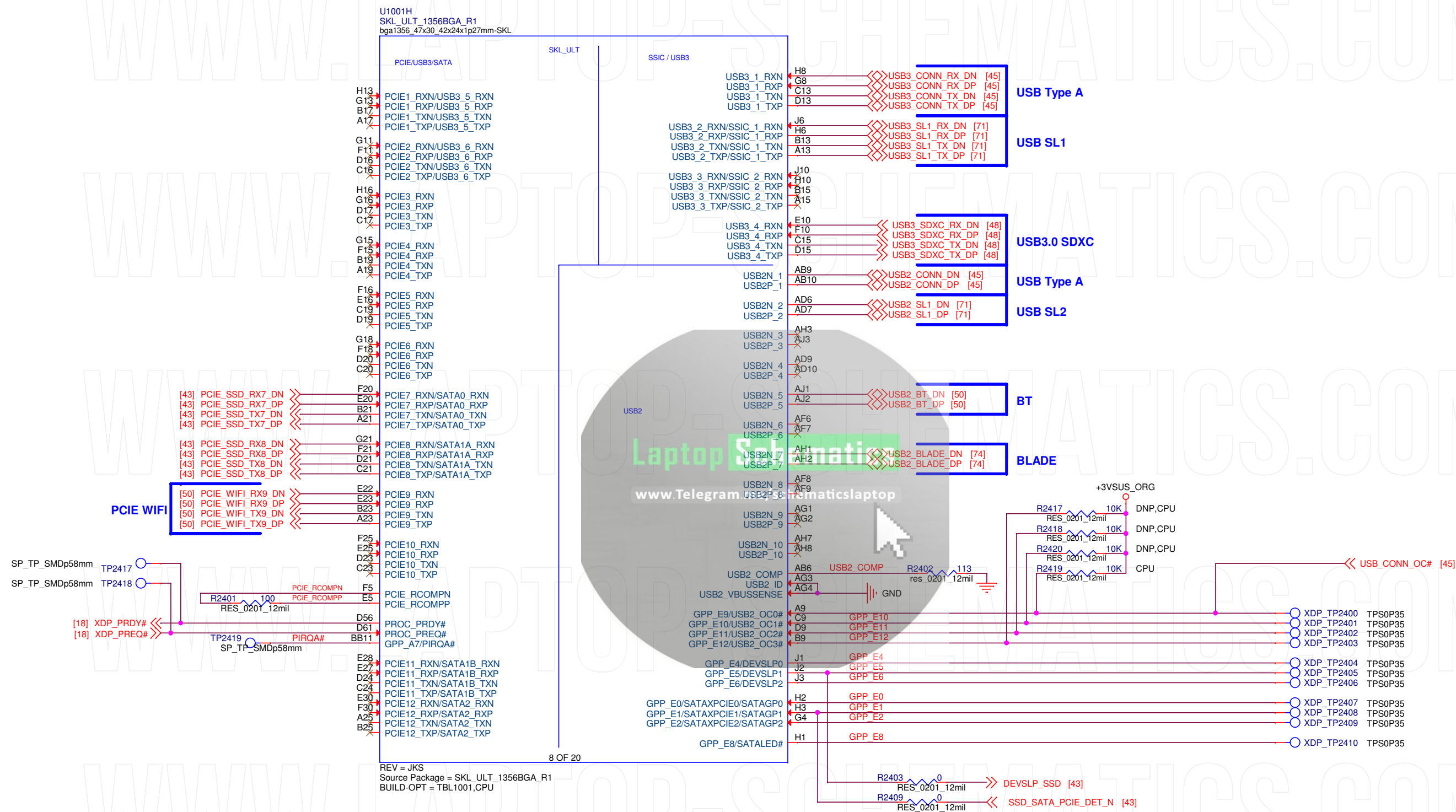
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

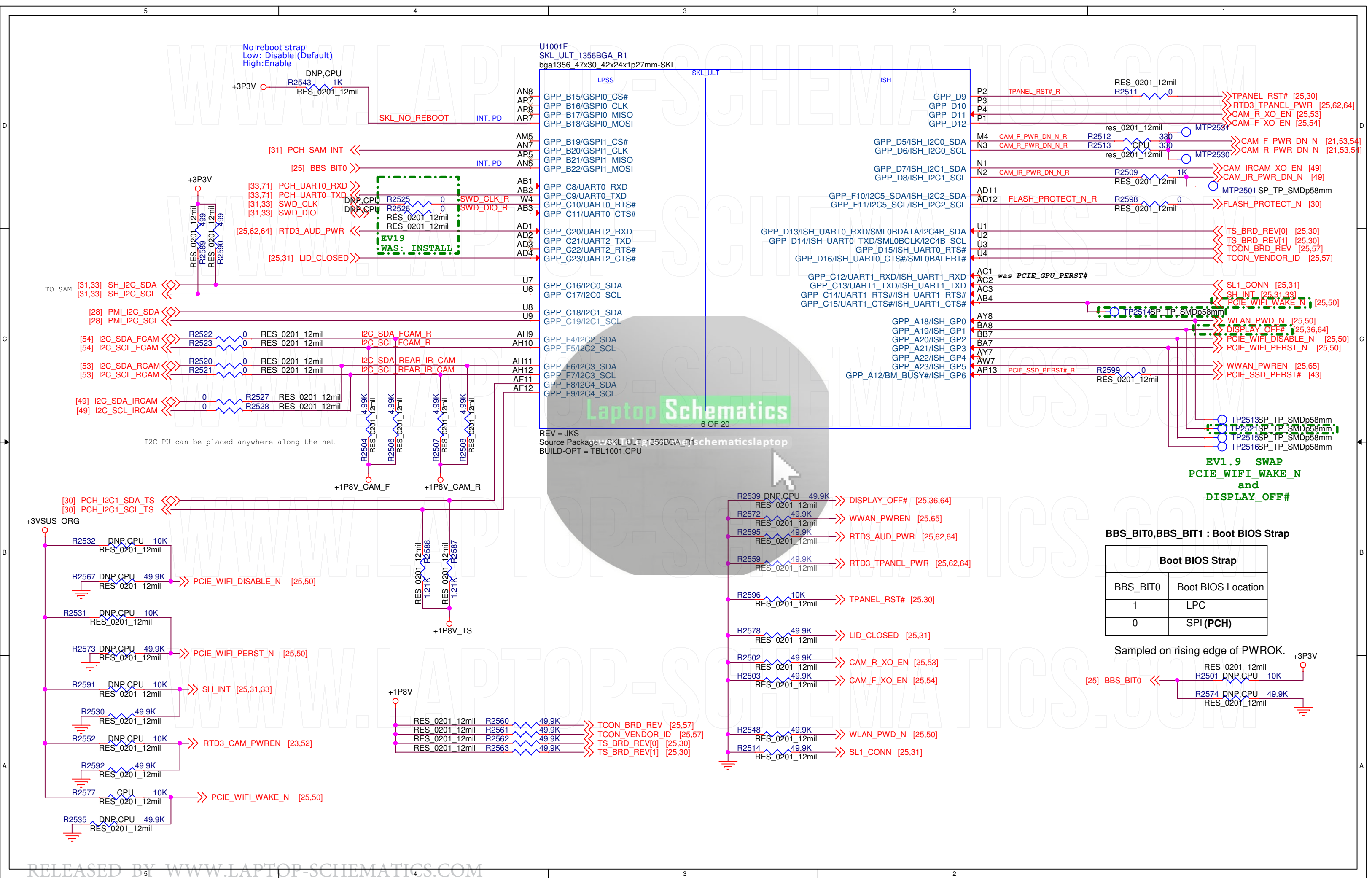


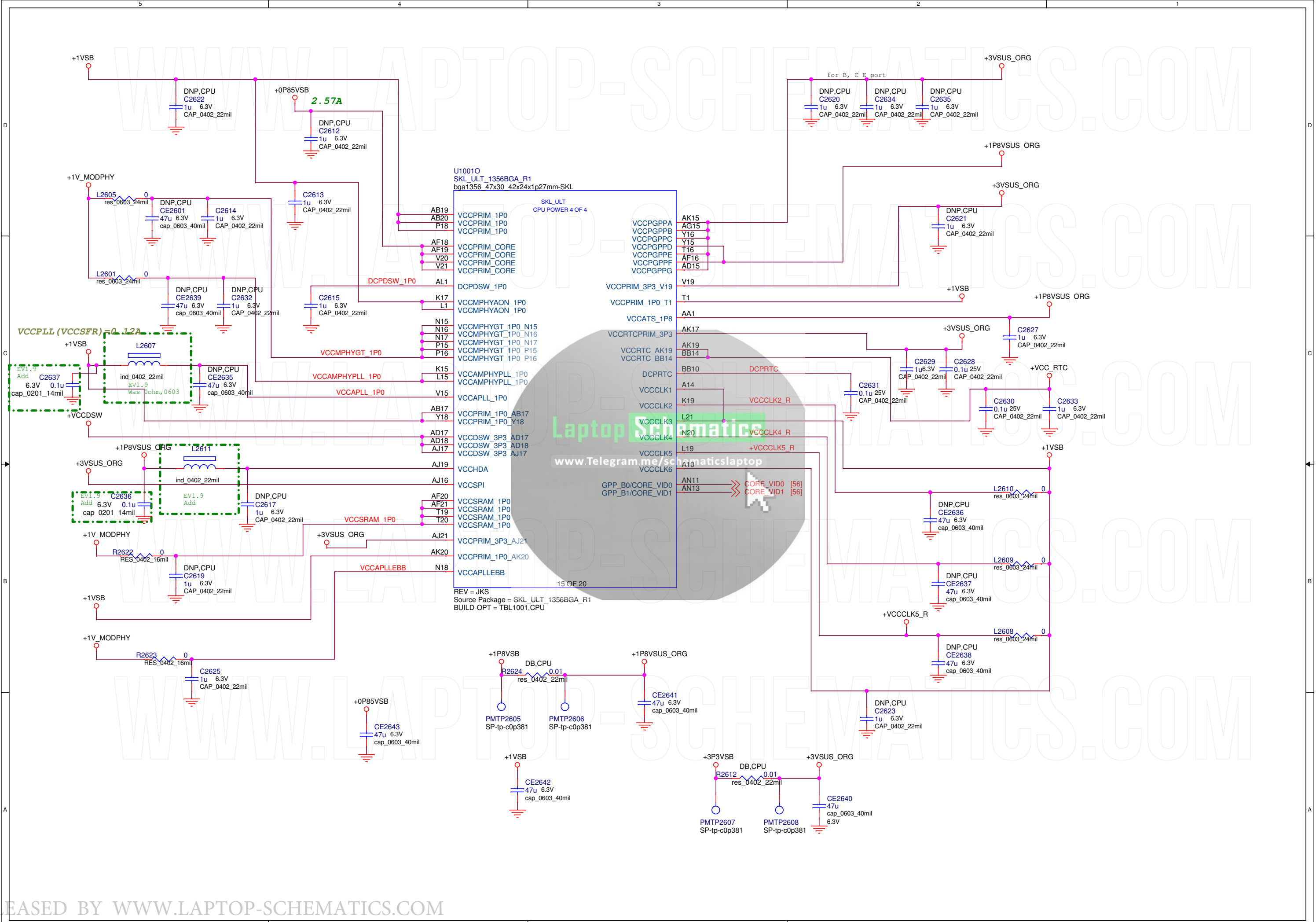


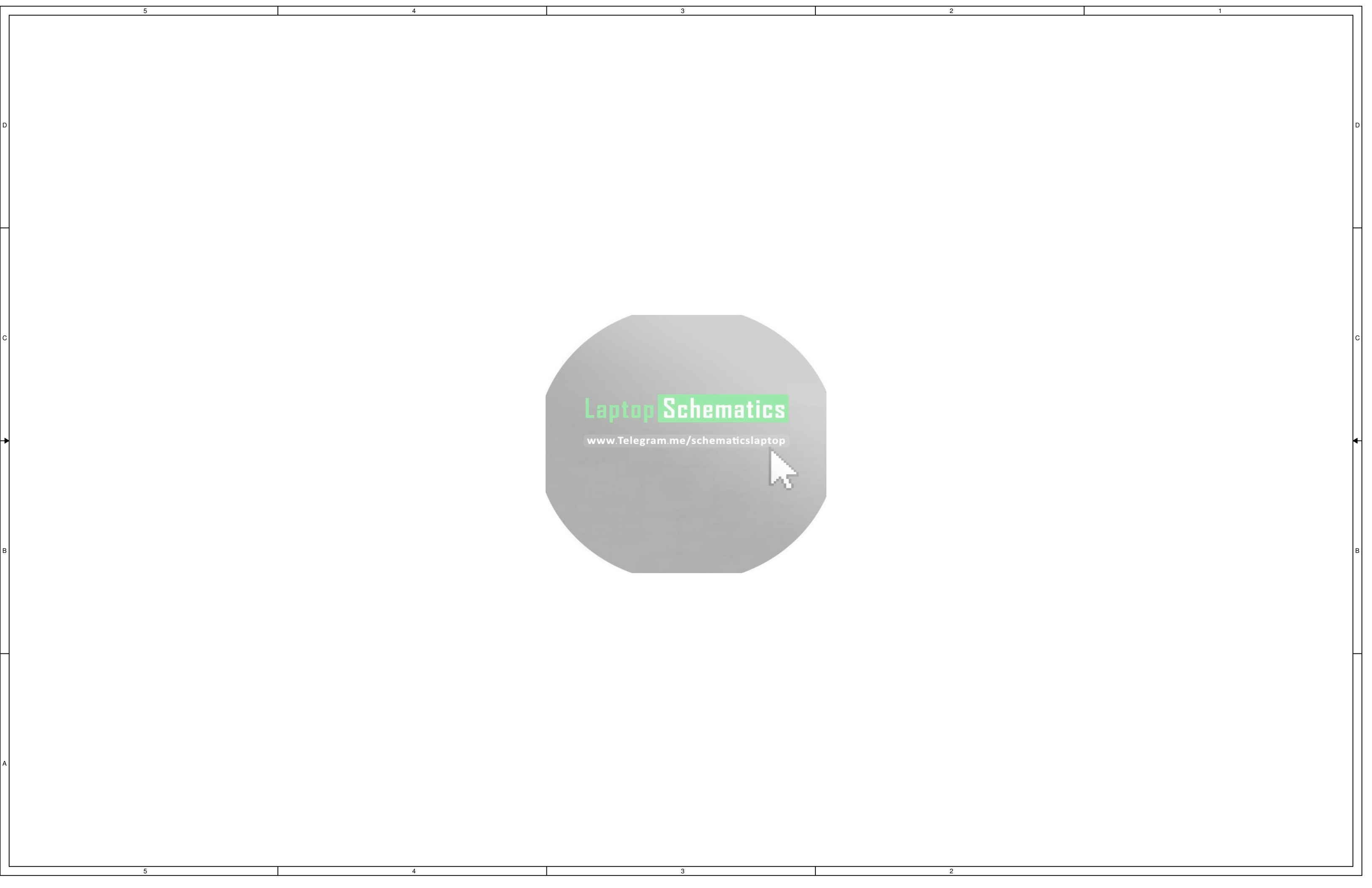






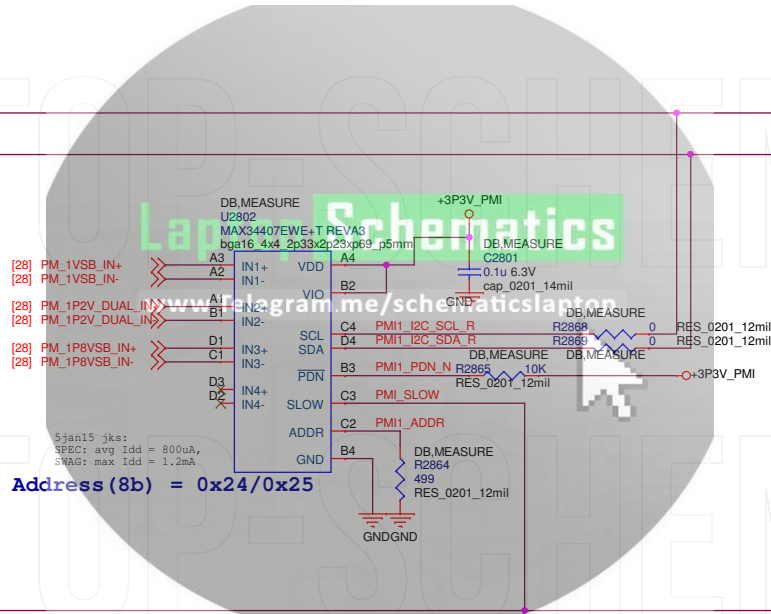
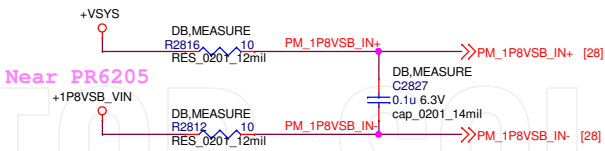
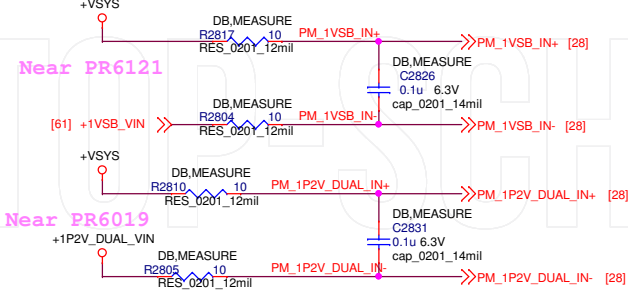
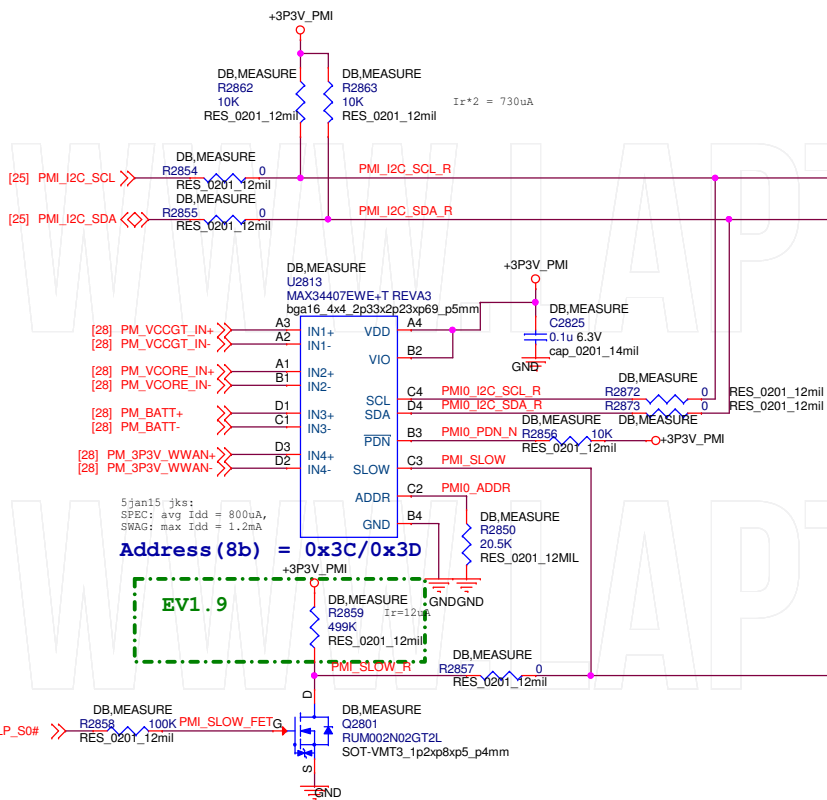
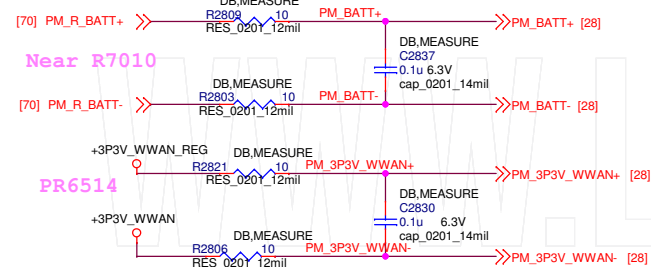
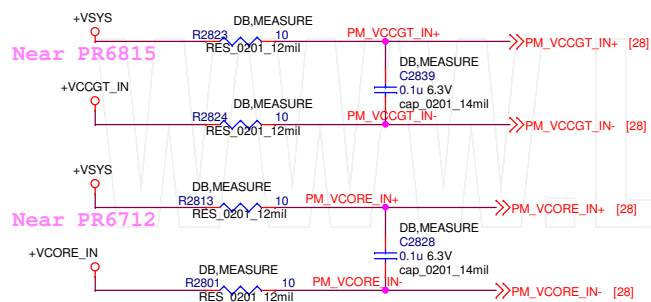






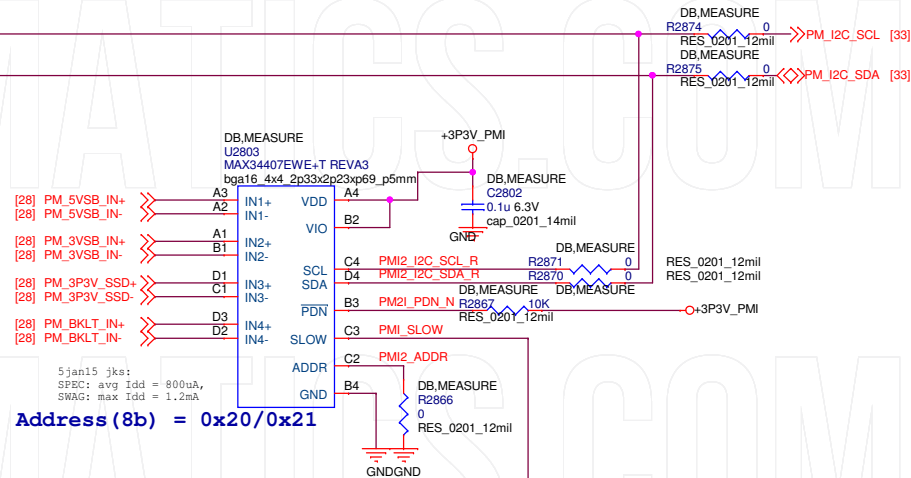
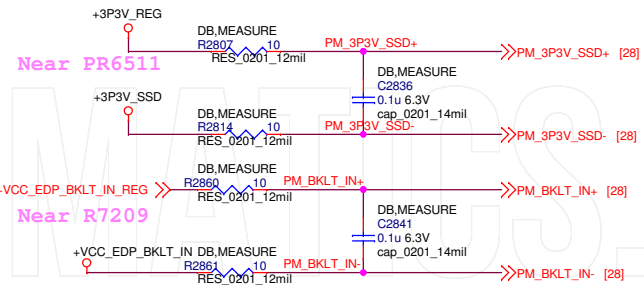
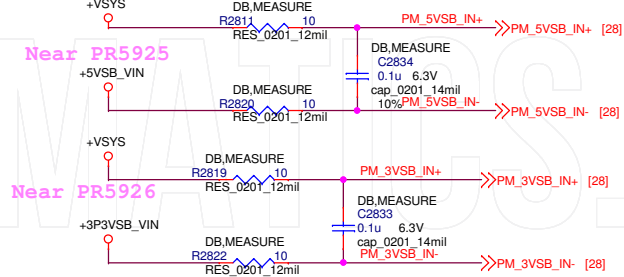
Laptop Schematics

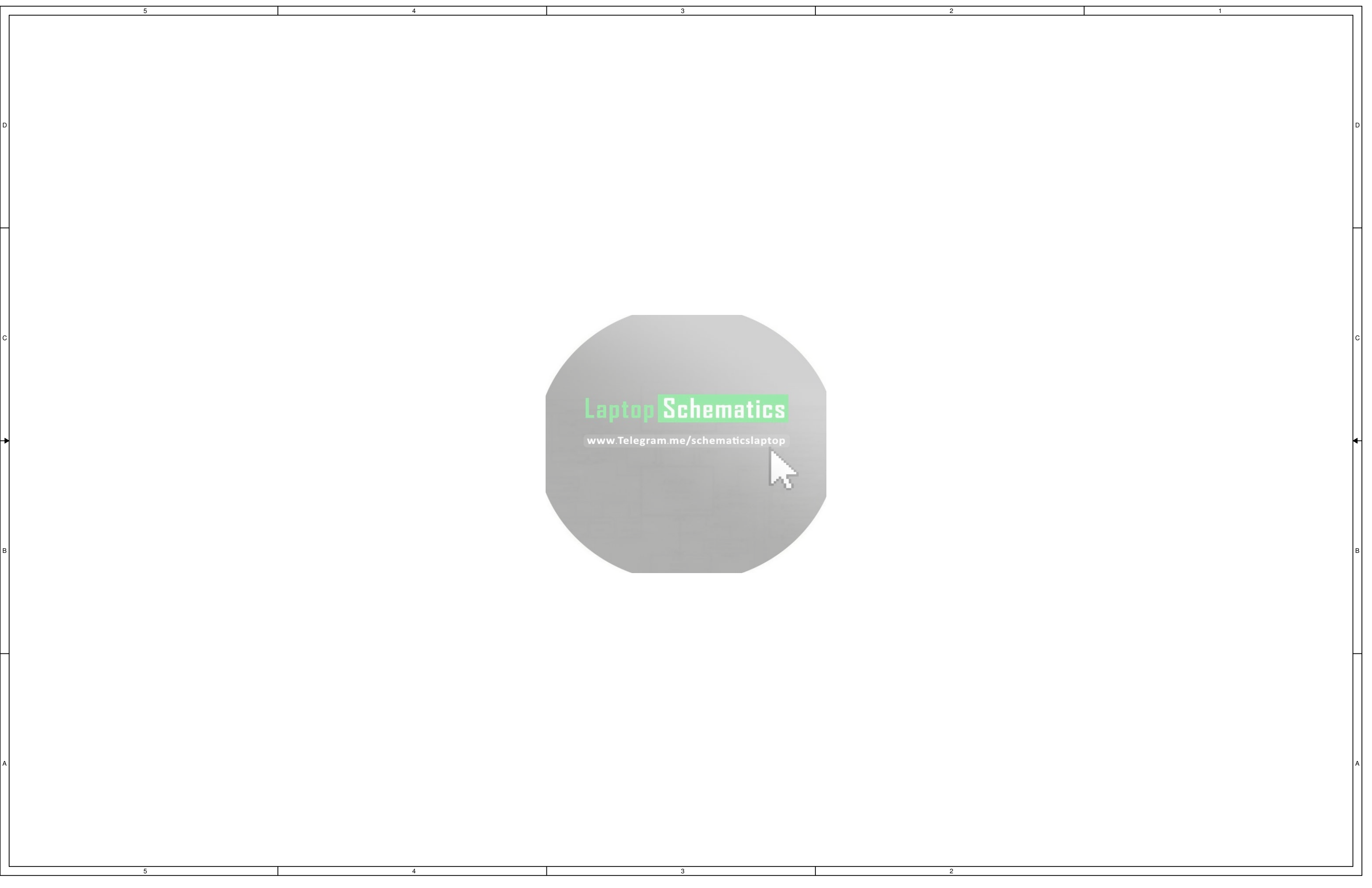
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Resistor Address for MAX3440

20.5K	=>	2x3C/2x3D
11.0K	=>	2x38/2x39
5.90K	=>	2x34/2x35
3.16K	=>	2x30/2x31
1.74K	=>	2x2C/2x2D
931K	=>	2x28/2x29
499	=>	2x24/2x25
GND	=>	2x20/2x21

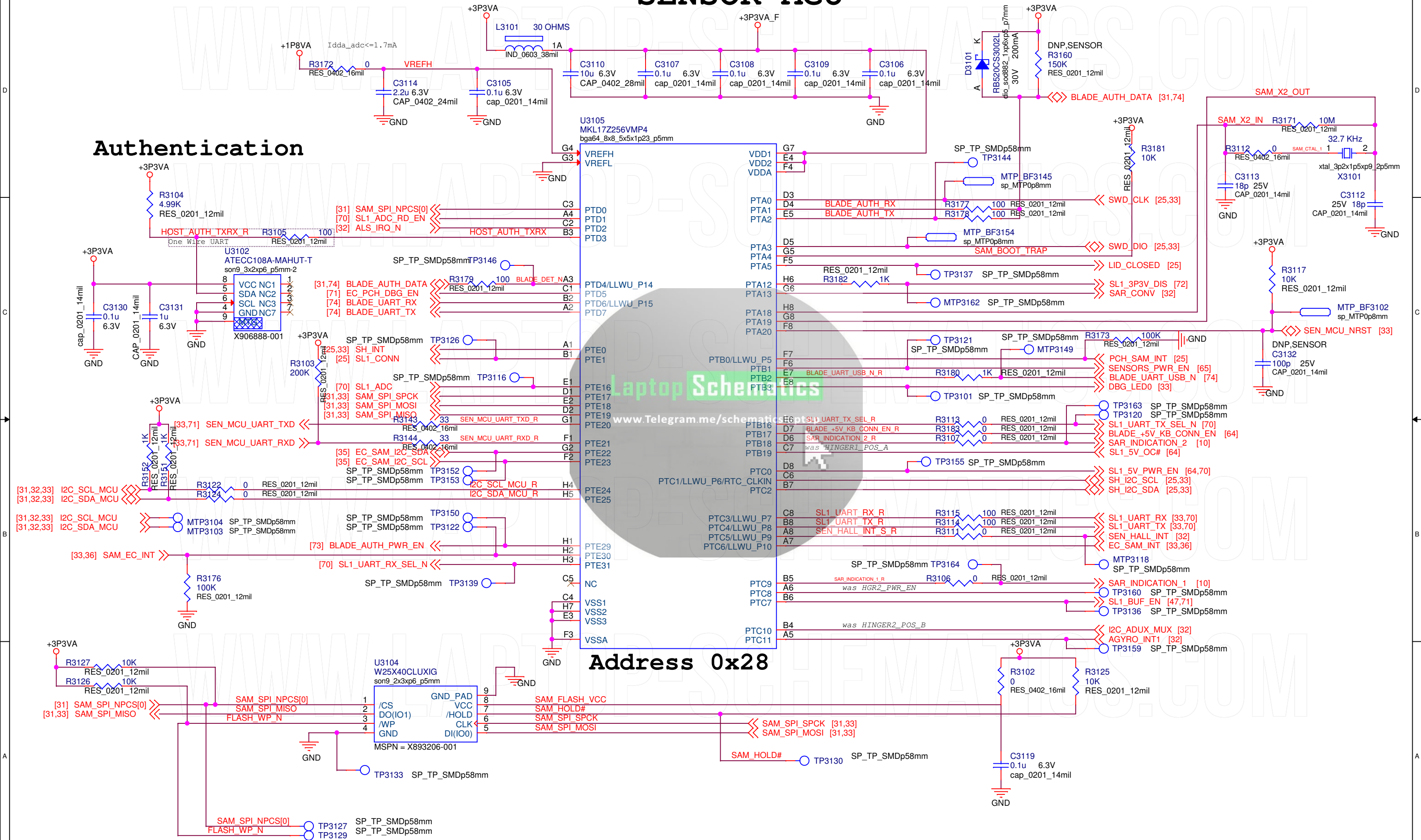




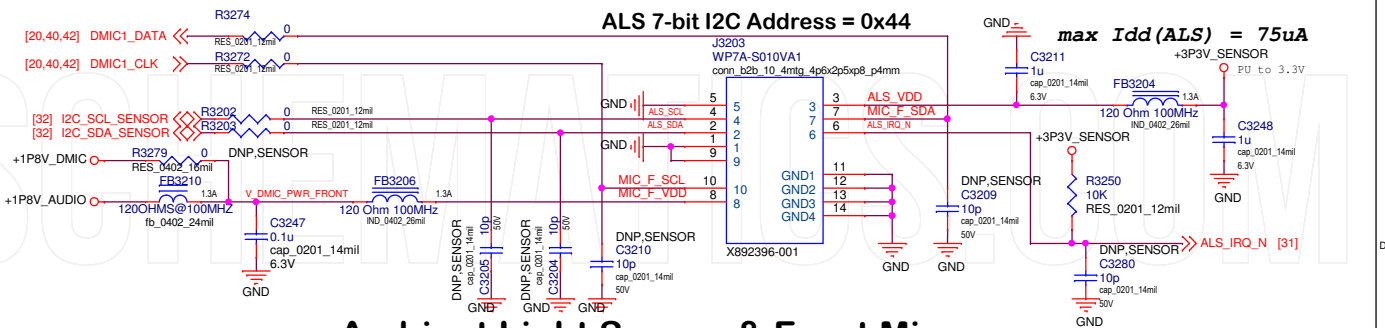
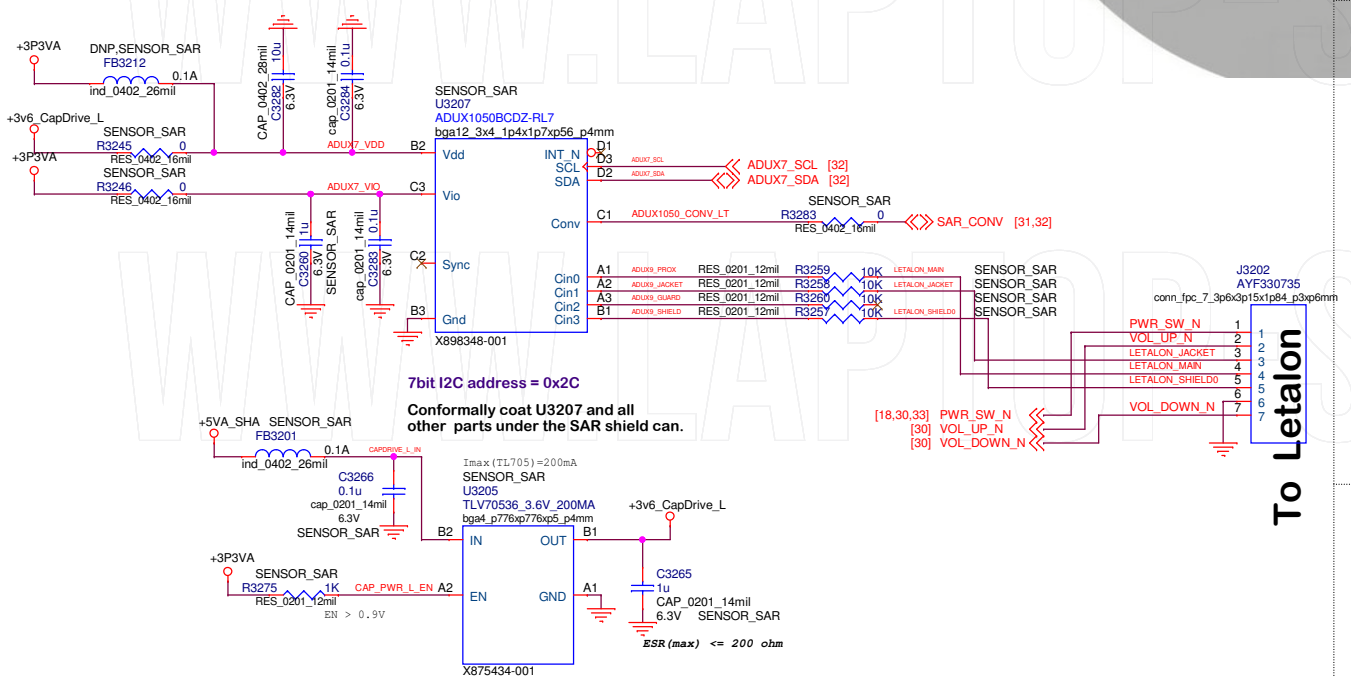
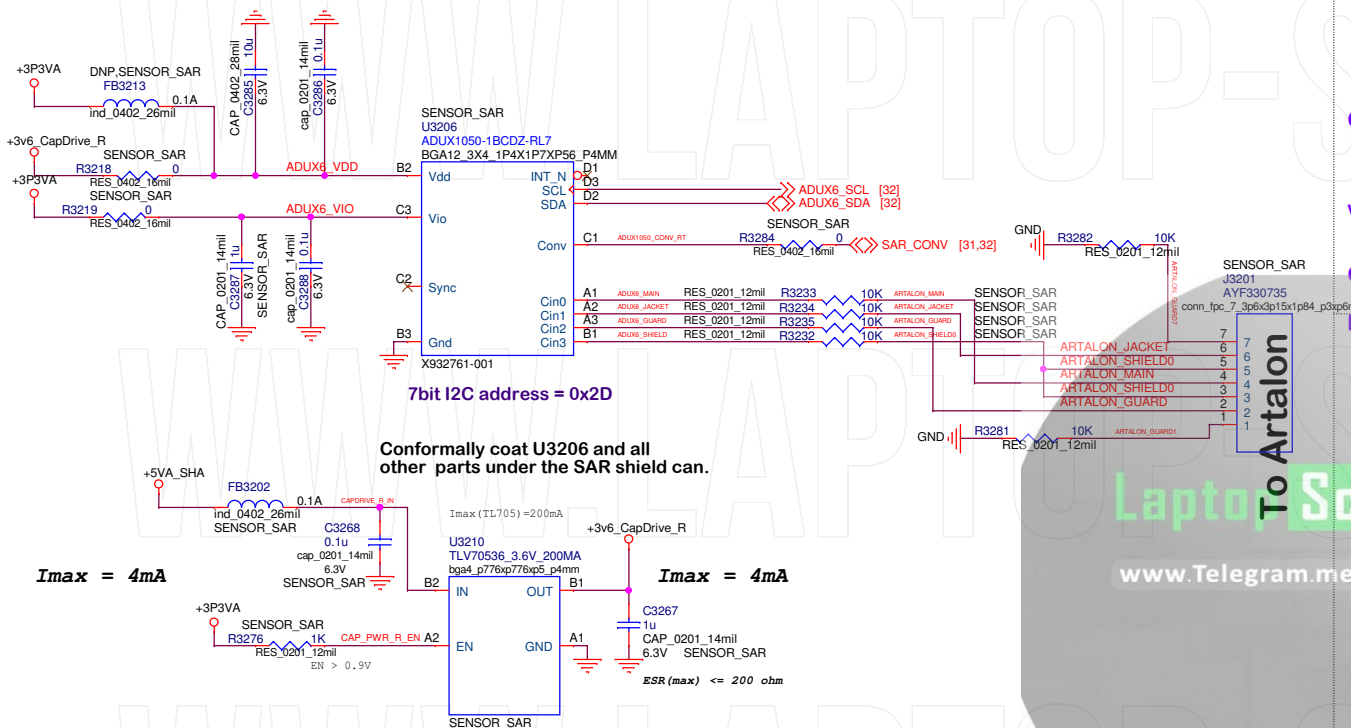
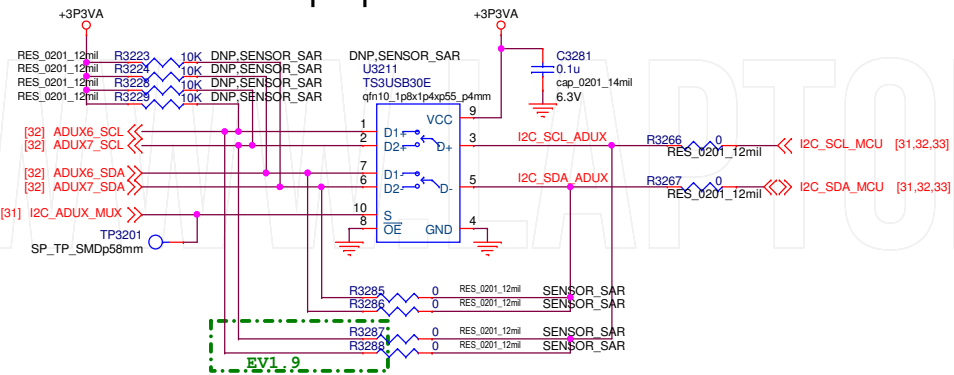
SENSOR MCU

Authentication

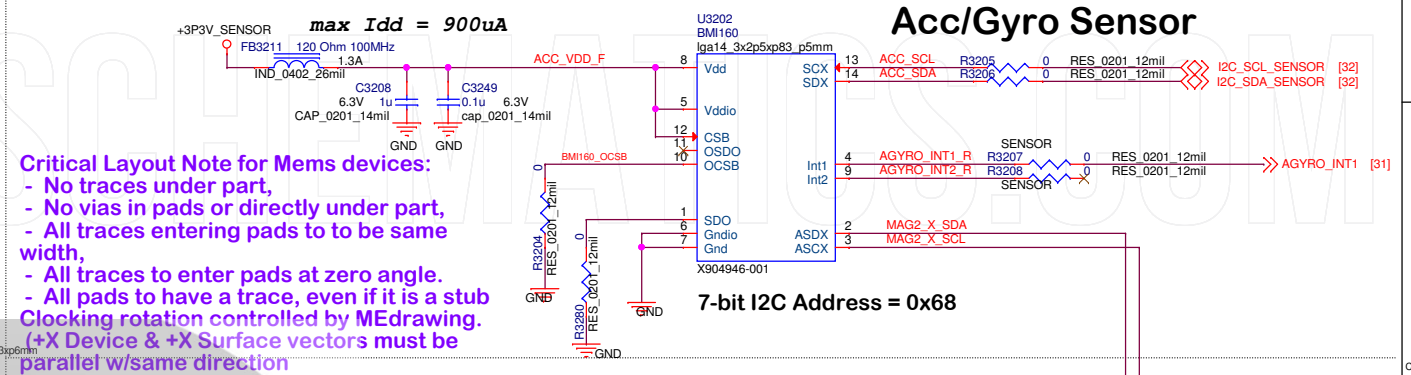
Address 0x28



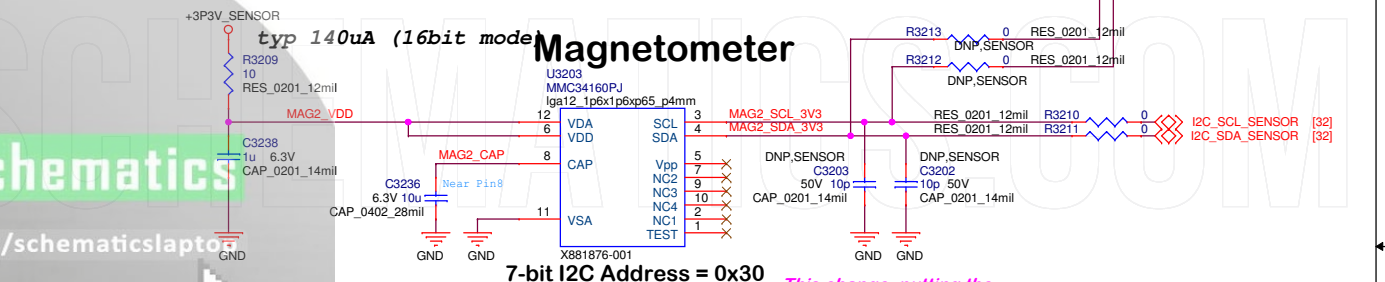
WiFi envelope protection drivers



Ambient Light Sensor & Front Mic



Acc/Gyro Sensor

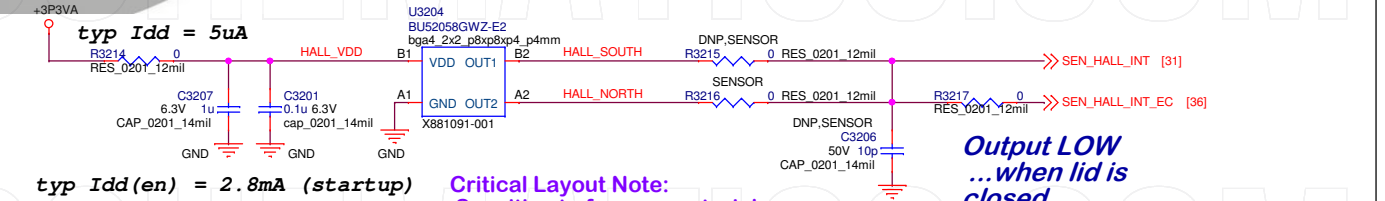


de Magnetometer

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by
MEdrawing.

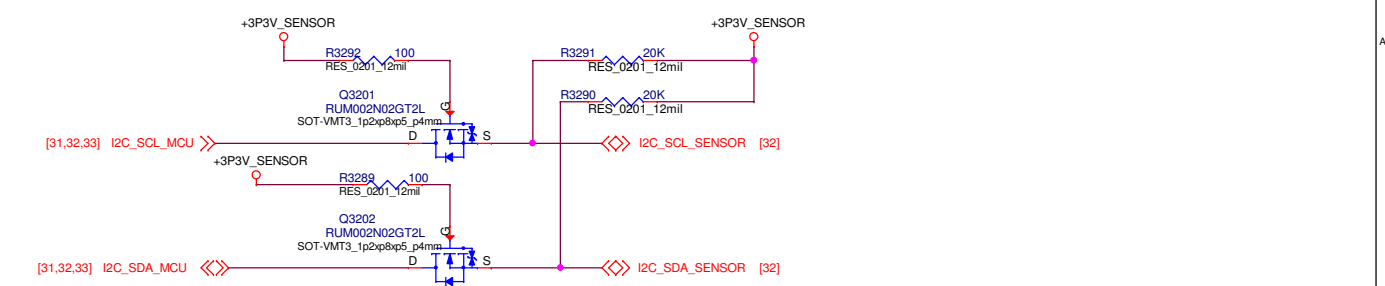
This change, putting the MAG behind the AGyro allows us to take advantage of the time-stamped FIFO in the AGyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.

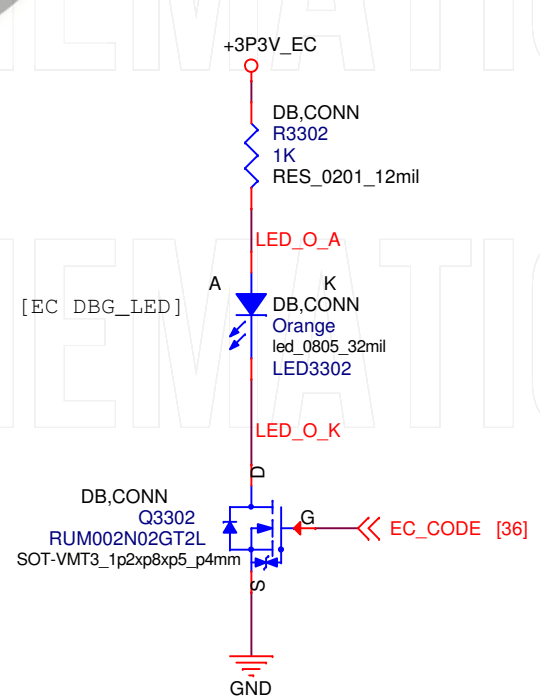
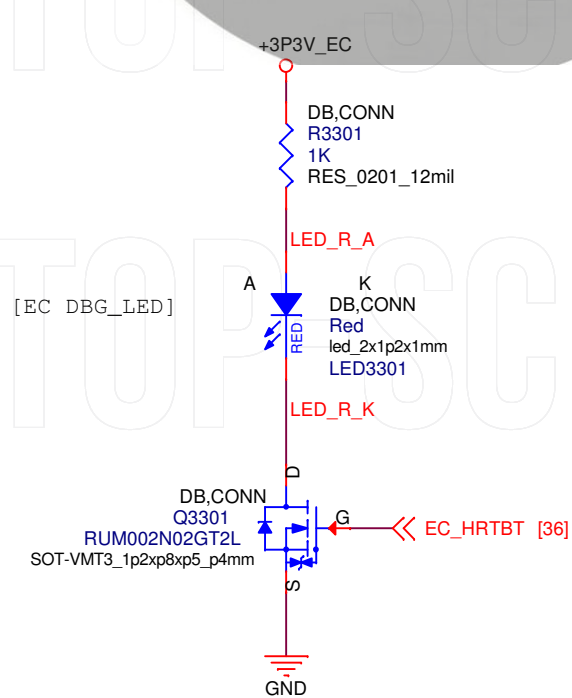
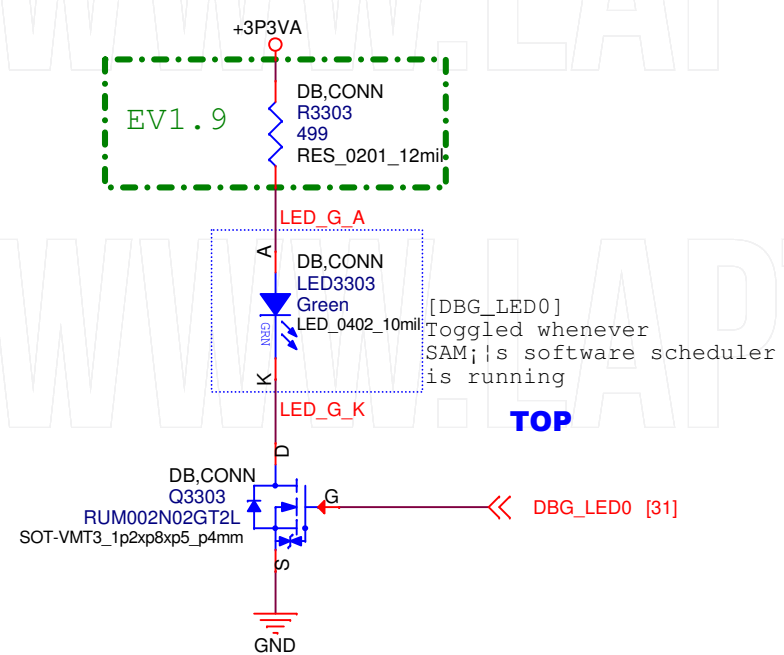
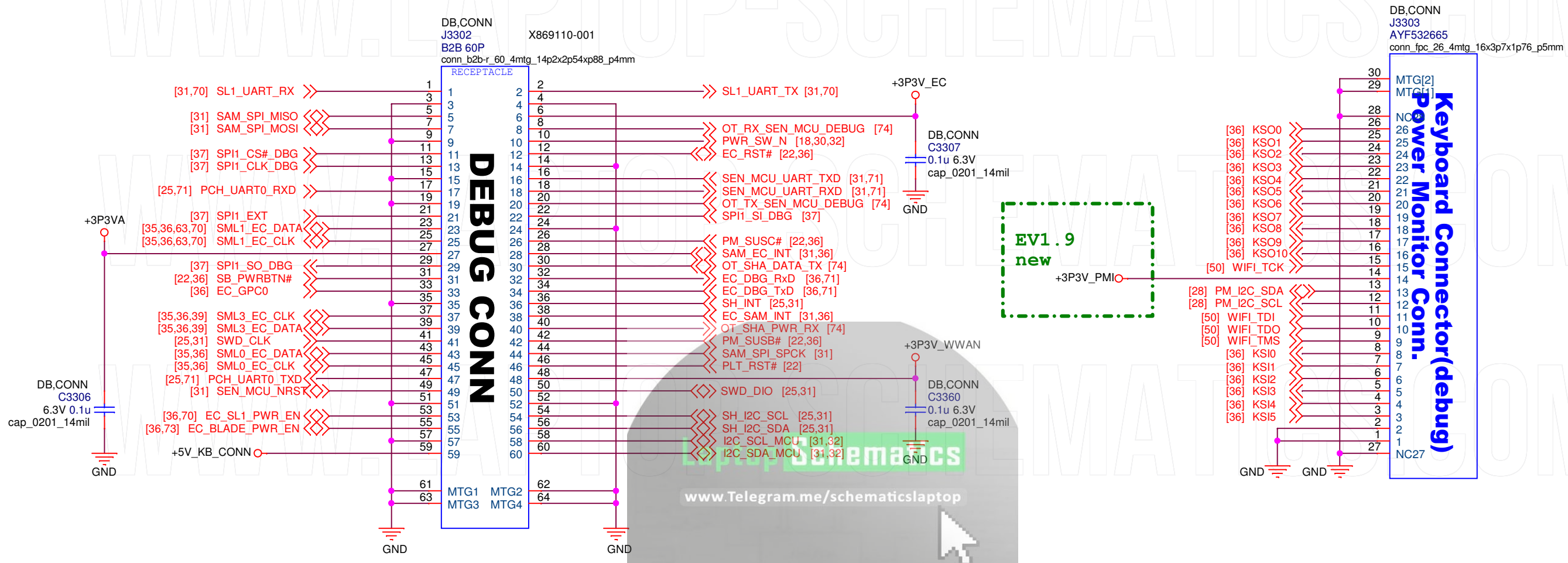
Hall Effect Sensor

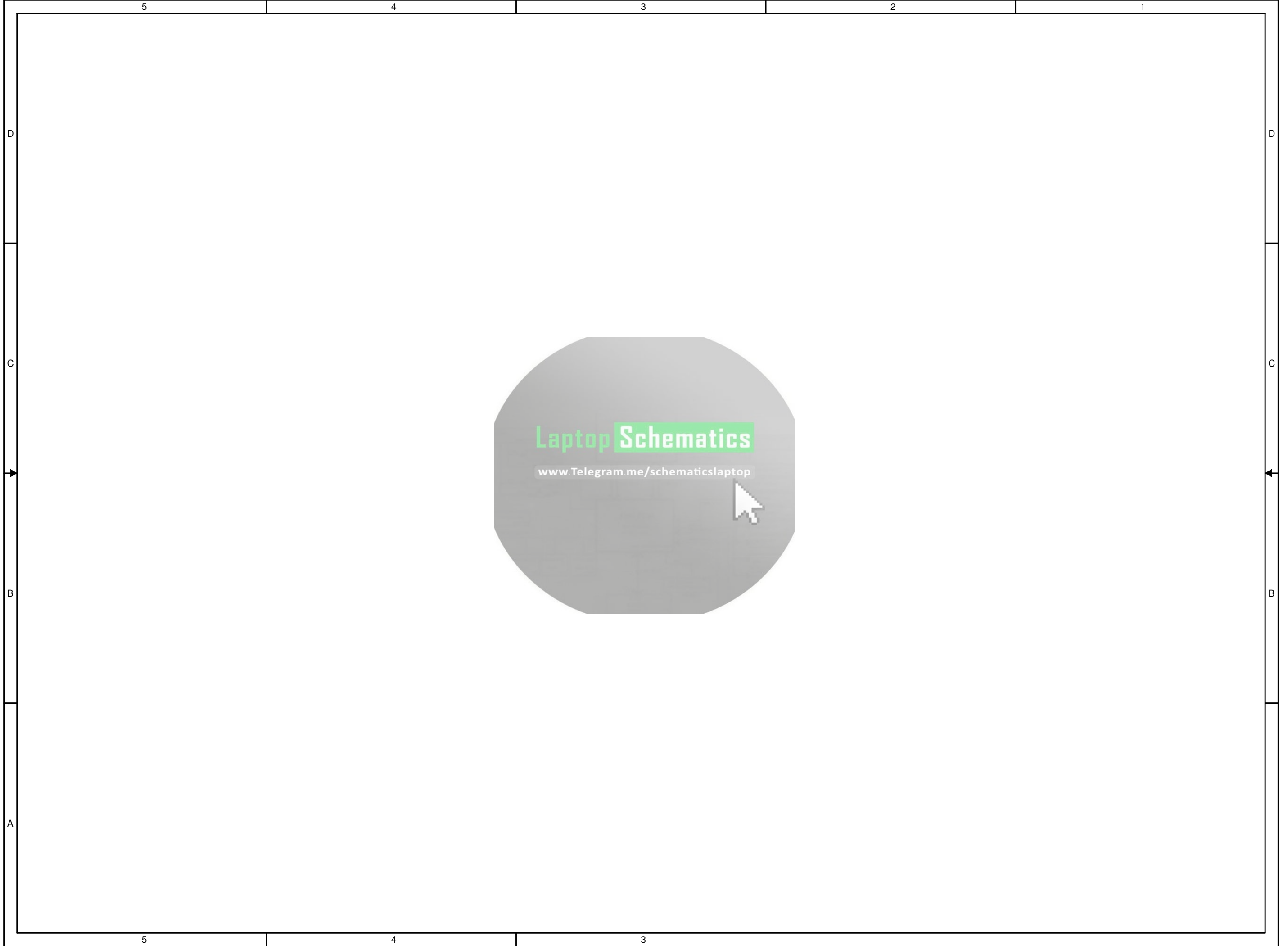


Output LOW
...when lid is closed

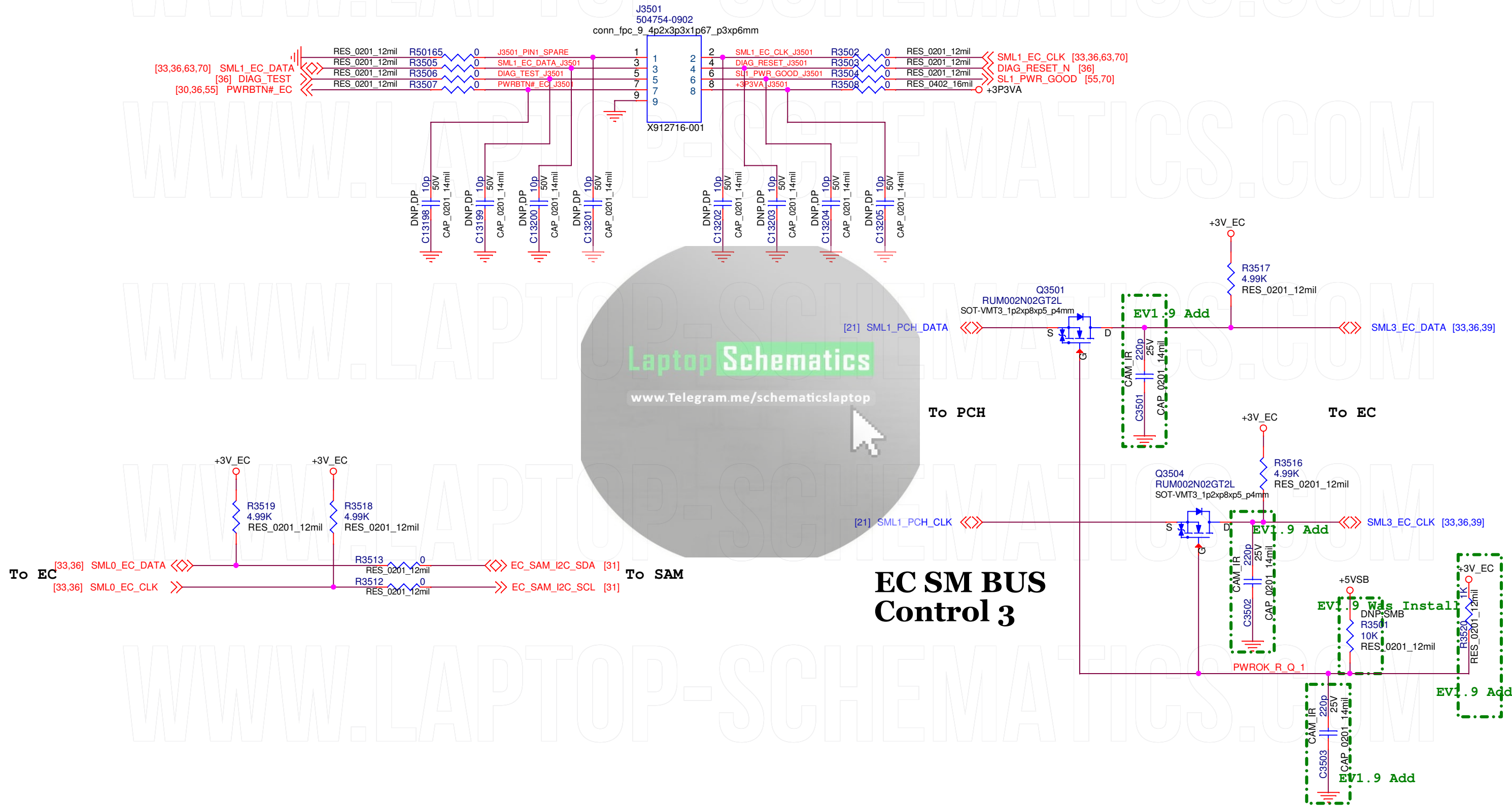
Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur
as early as 30Gauss North B-field
or as late as 50Gauss North B-field
Be careful not to mount within 15mm
of speaker autofocus camera or other
magnet.
X-Y location controlled by MEdrawing.

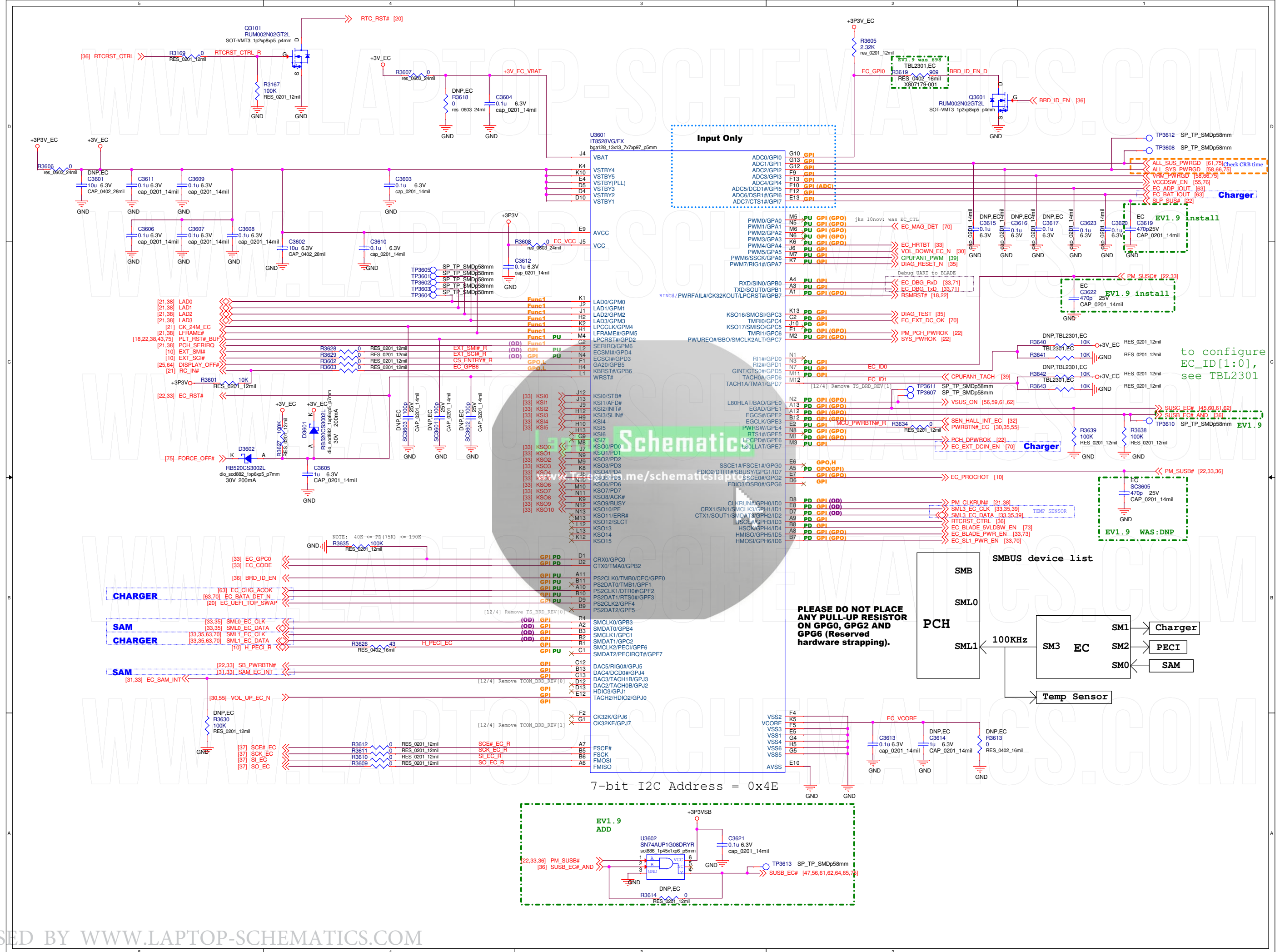






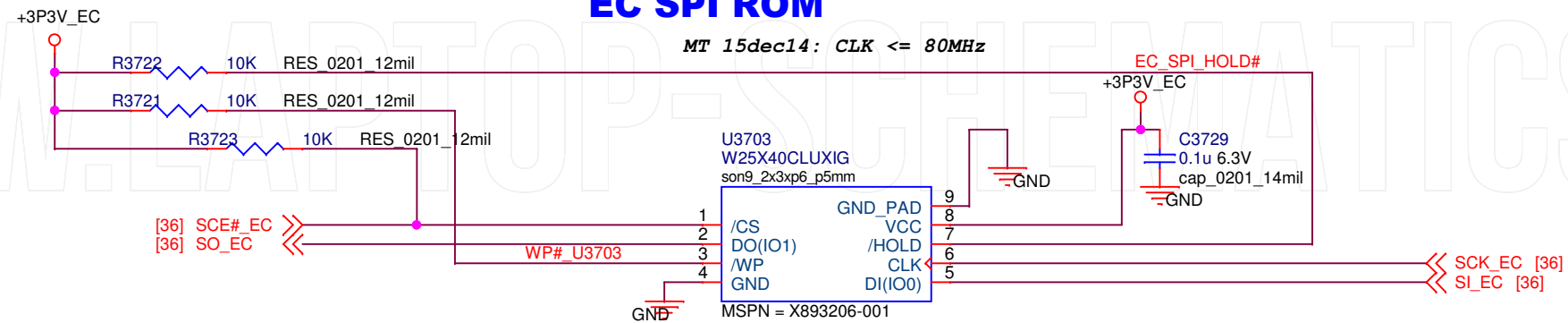
DIAGNOSTIC CONNECTOR





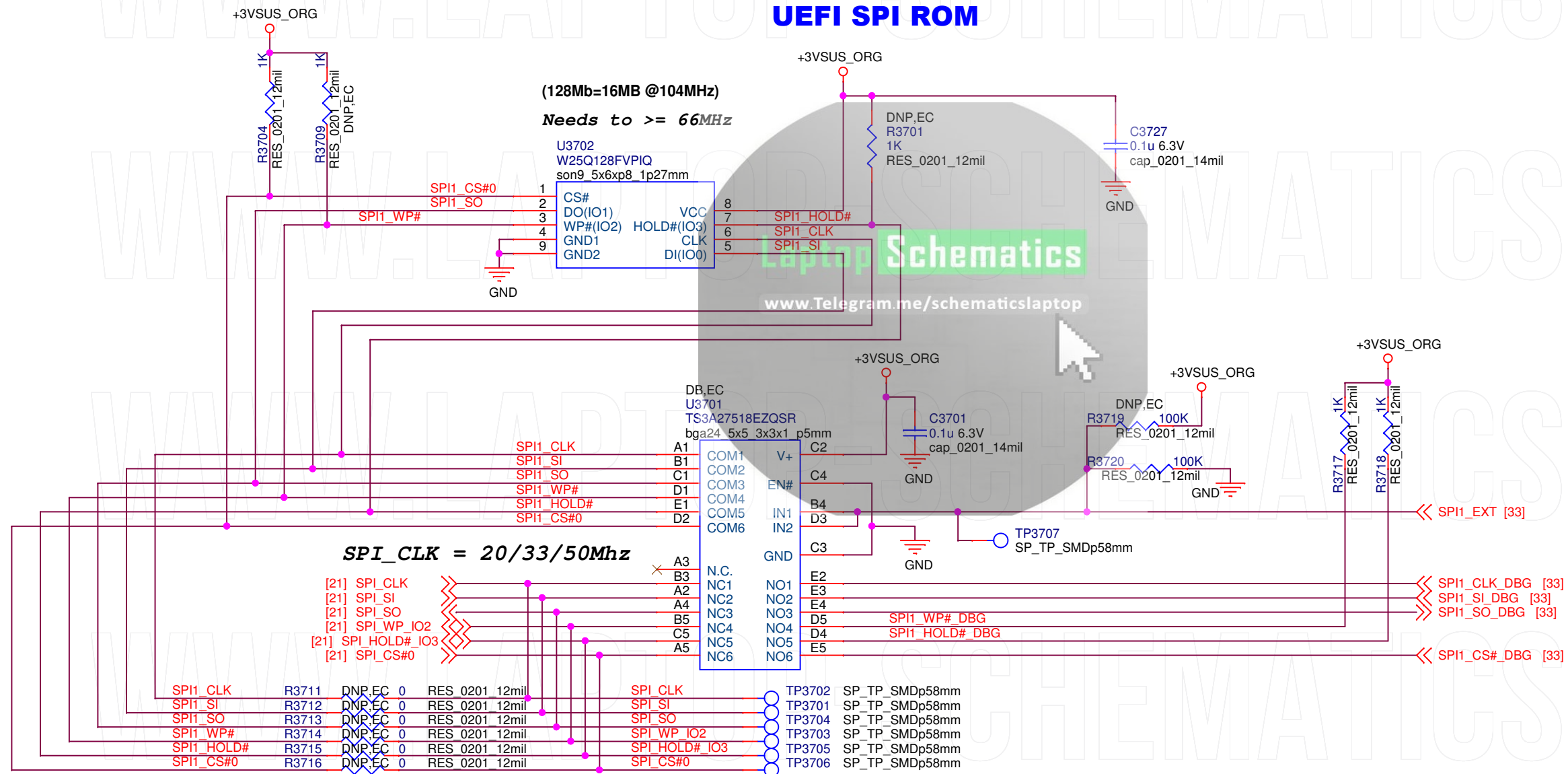
EC SPI ROM

```
MT 15dec14: CLK <= 80MHz
```



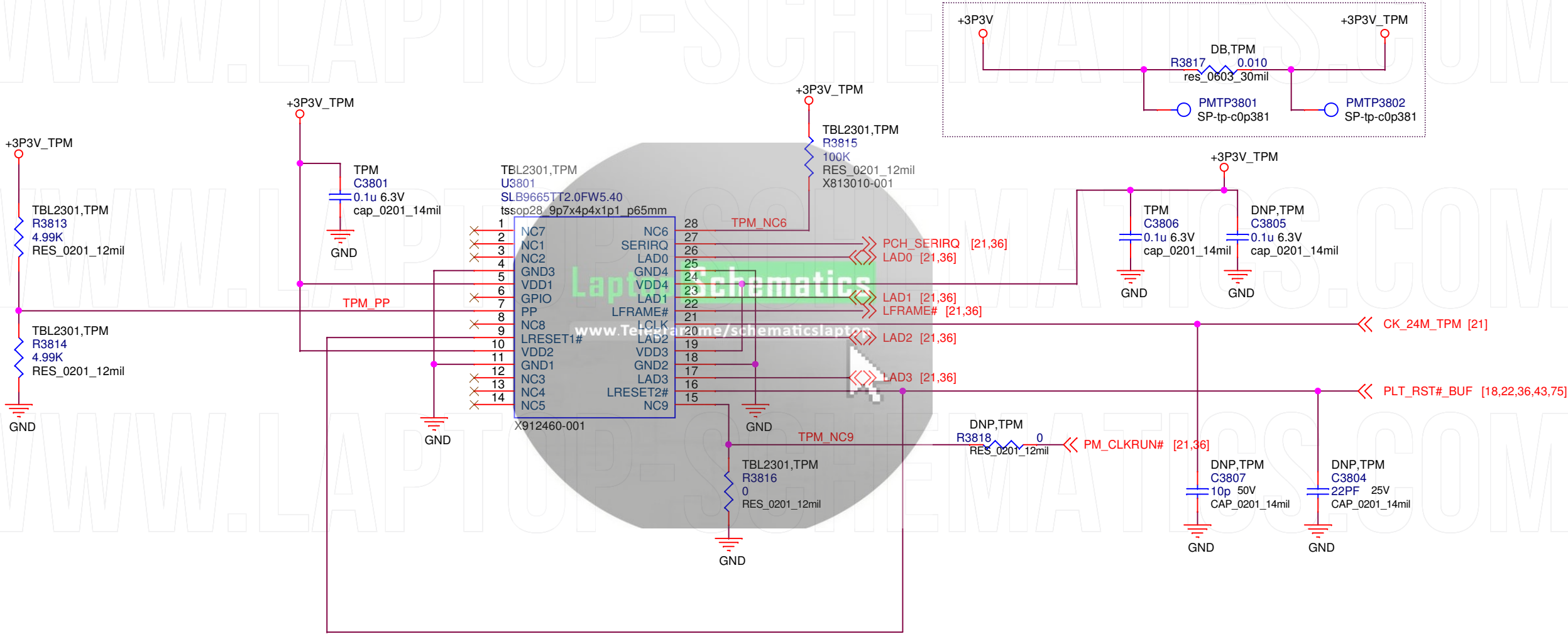
UEFI SPI ROM

Needs to $\geq 66\text{MHz}$



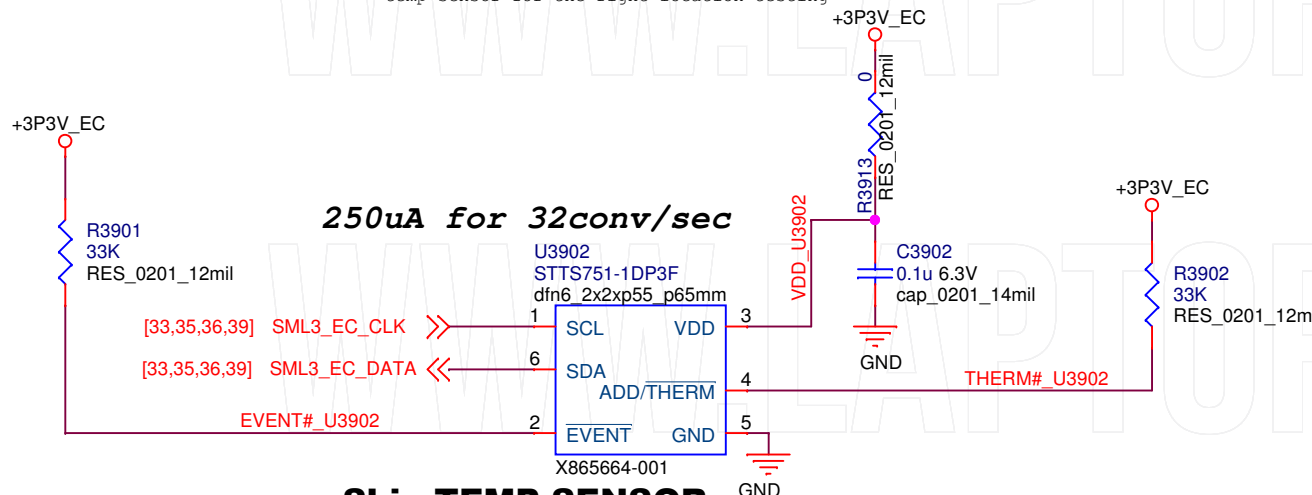
IN1/IN2 = L => COM to NC
IN1/IN2 = H => NC to COM

Trusted Platform Module



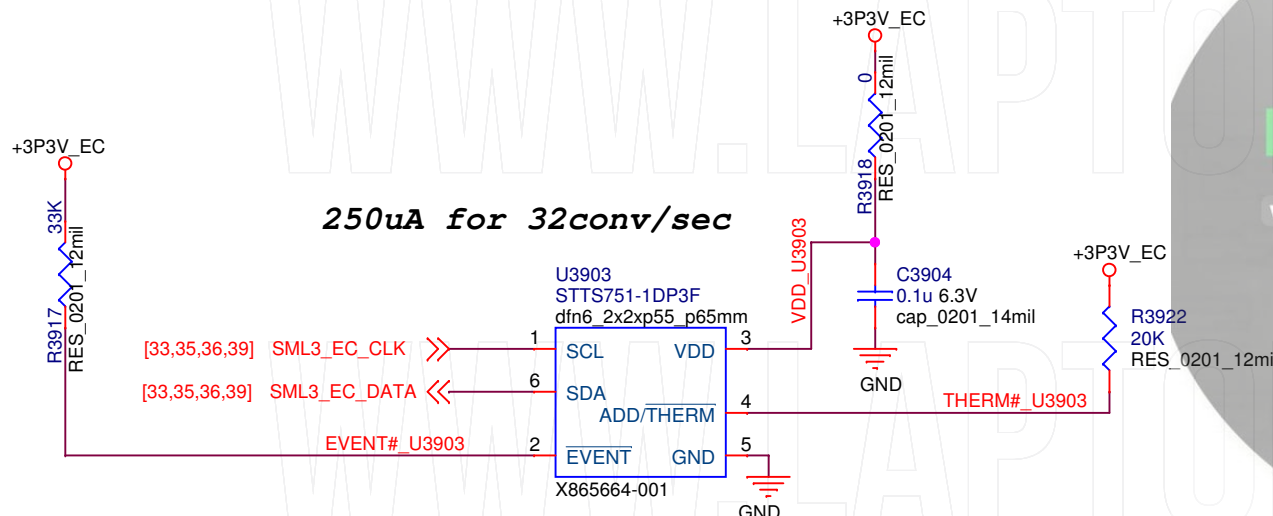
```
jks 6dec14: Only one sensor will be used for final product
```

temp sensor for the right location testing



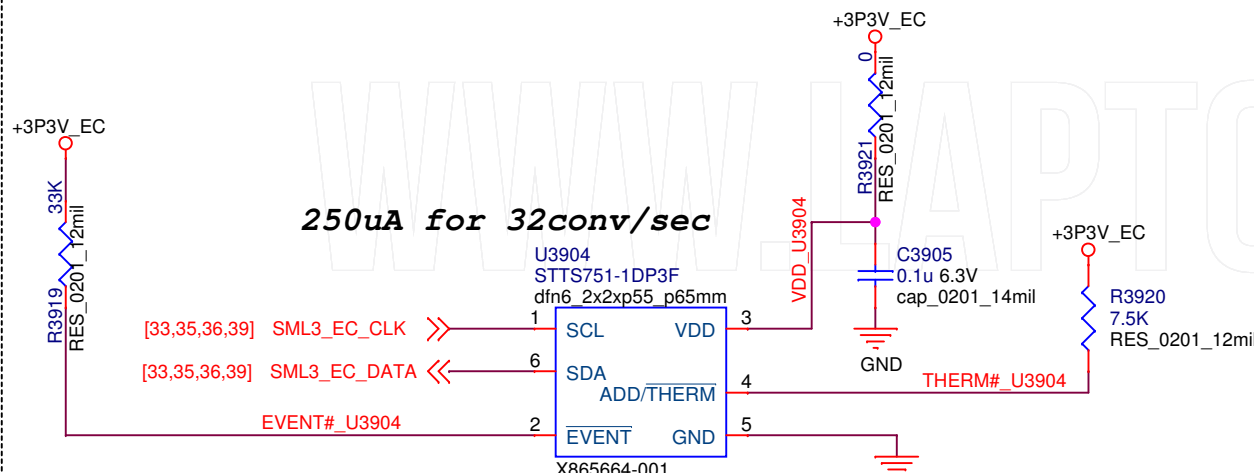
Skin TEMP SENSOR

7-bit I2C Address = 0x3E



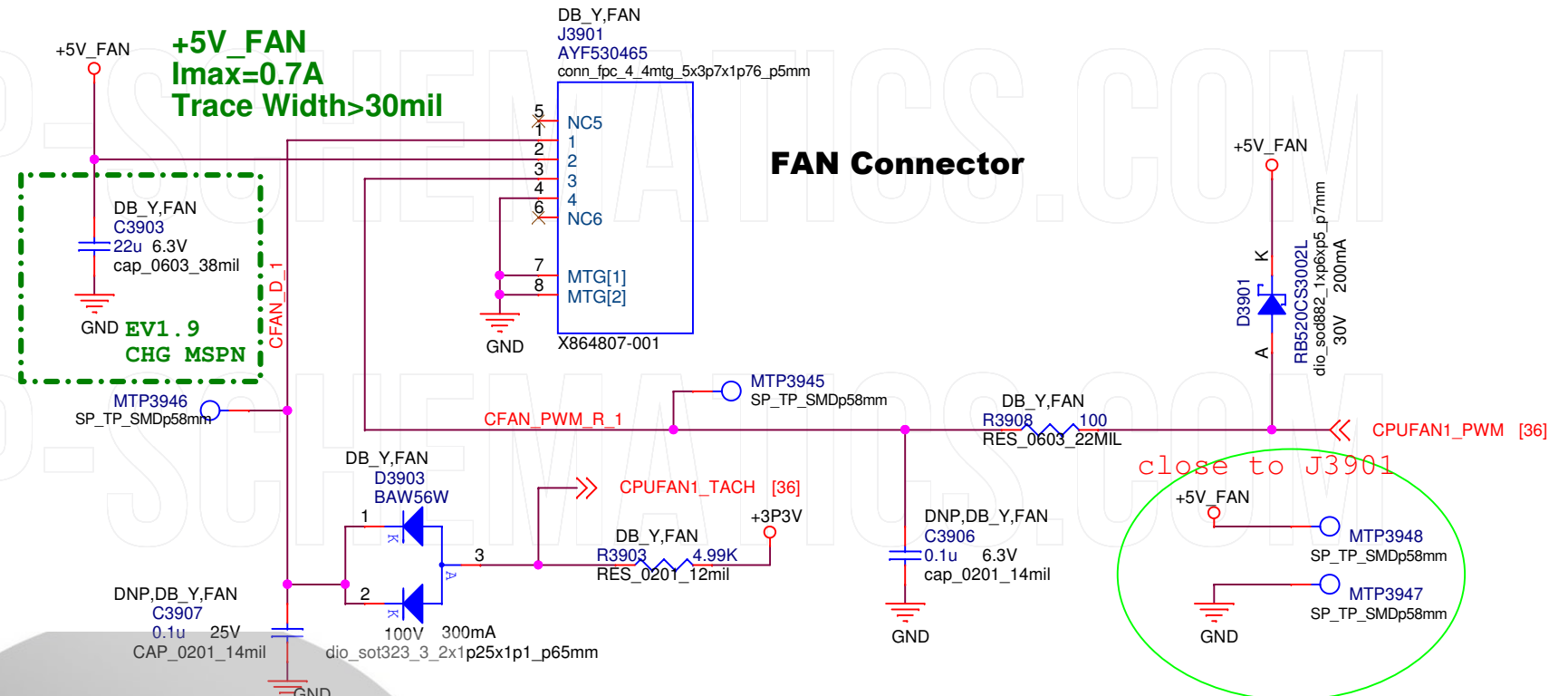
Skin TEMP SENSOR

7-bit I2C Address = 0x3A



Skin TEMP SENSOR

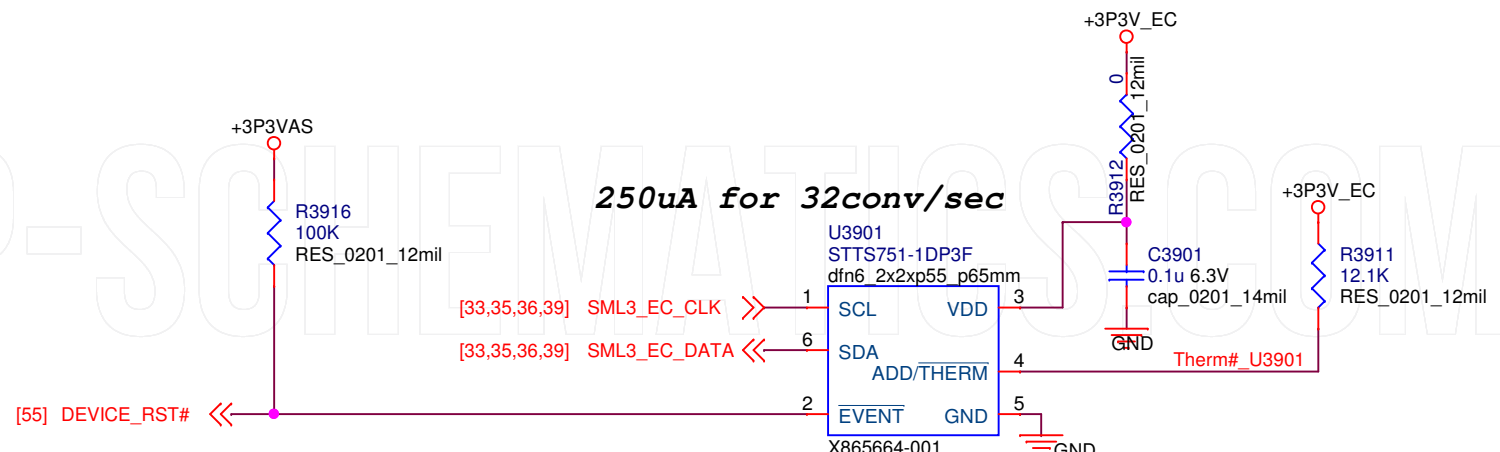
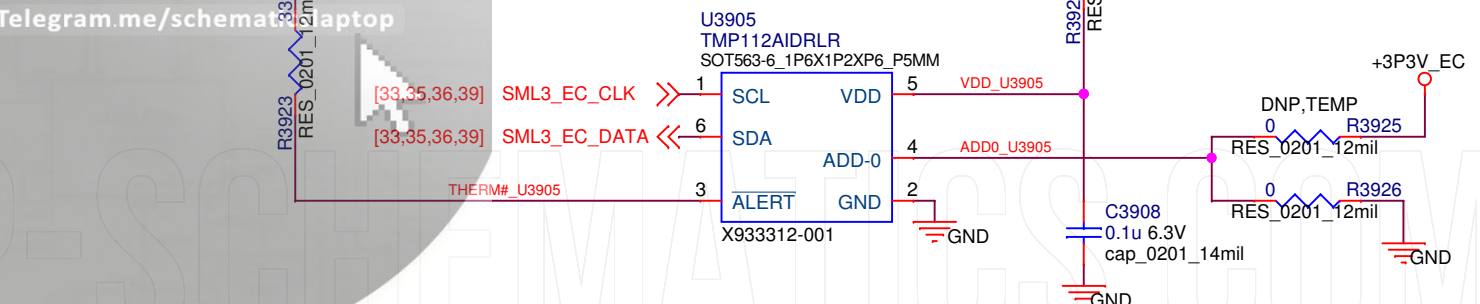
7-bit I2C Address = 0x 4A



FAN Connector

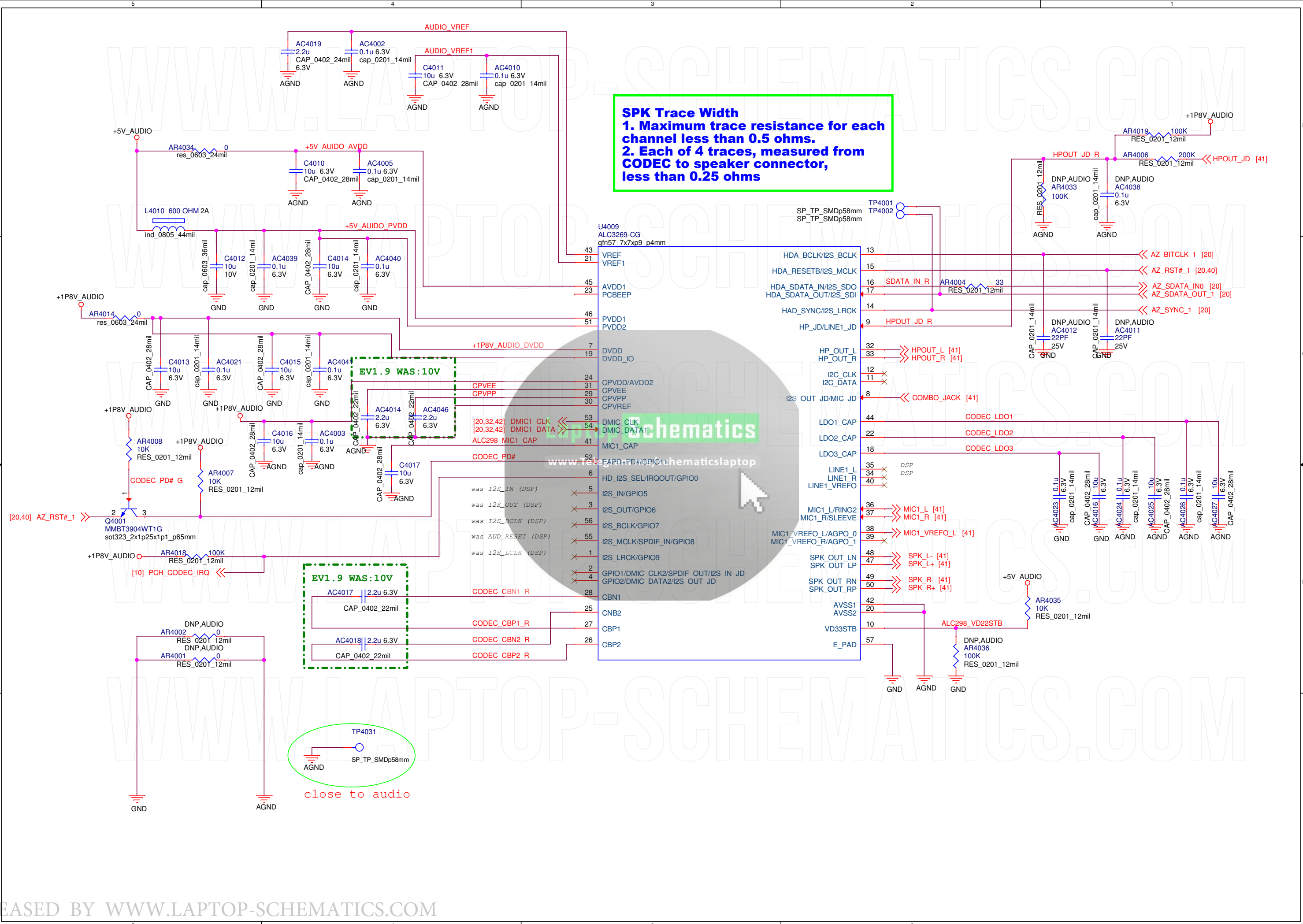
close to J3901

7-bit I2C Address = 0x48

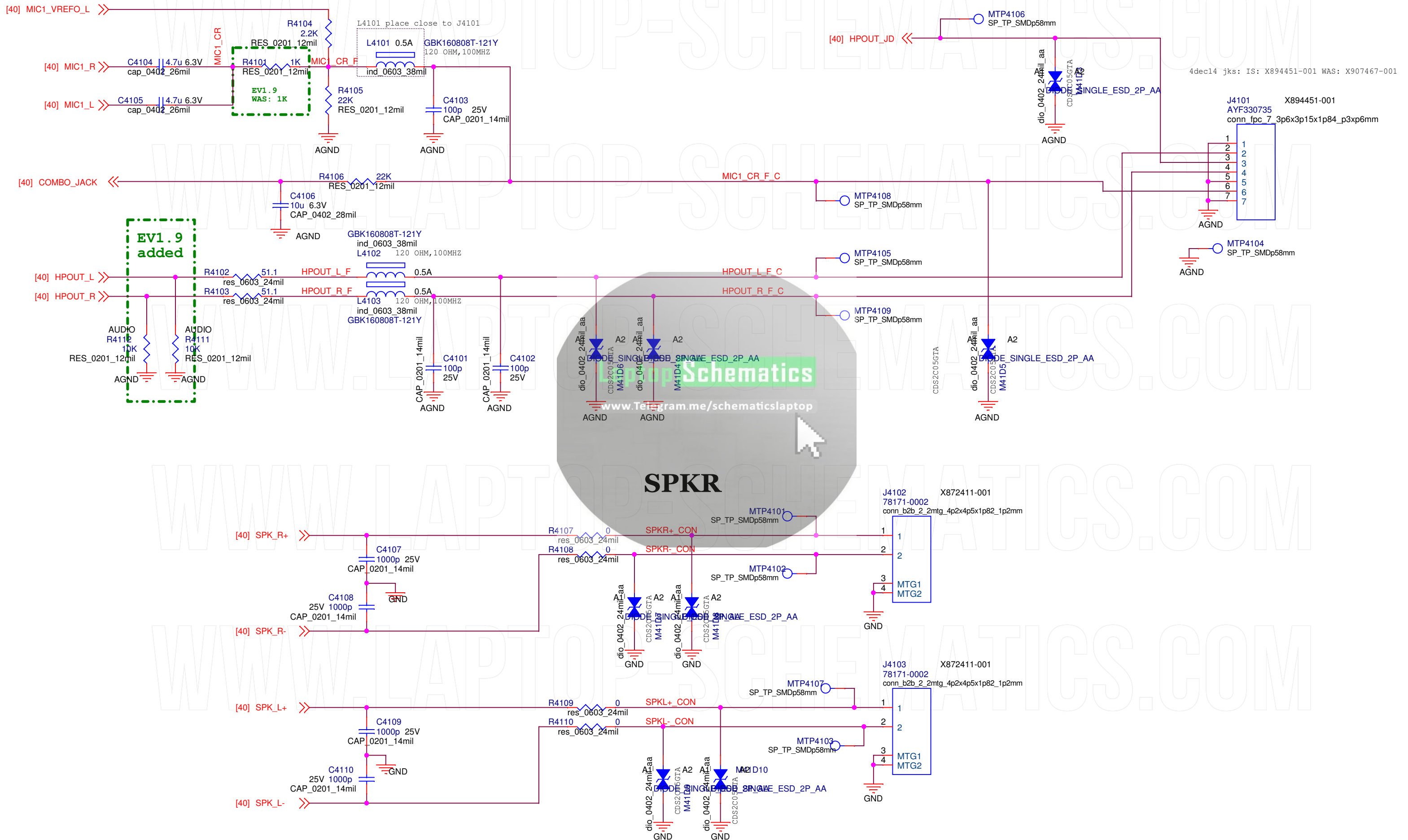


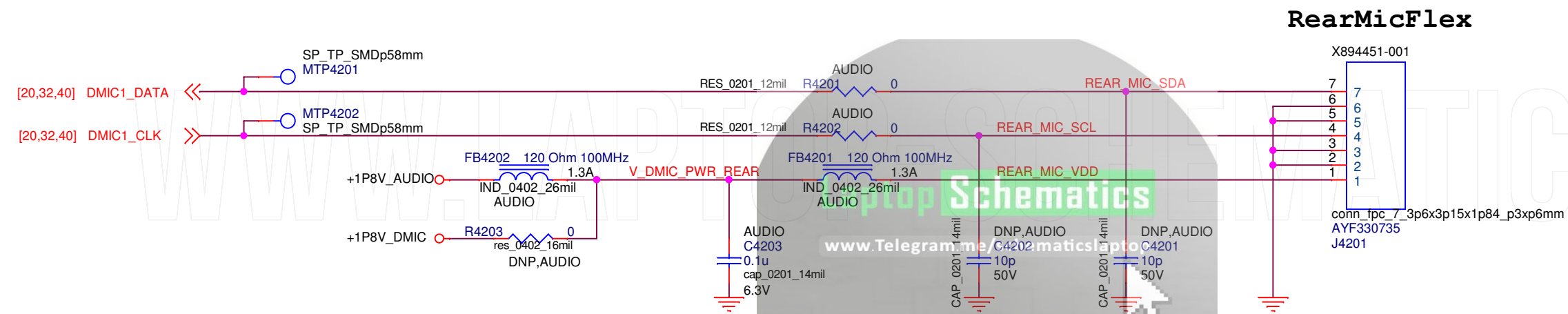
Surrend TEMP SENSOR

7-bit I2C Address = 0x4E



Audio Jack/MIC1 Combo Jack

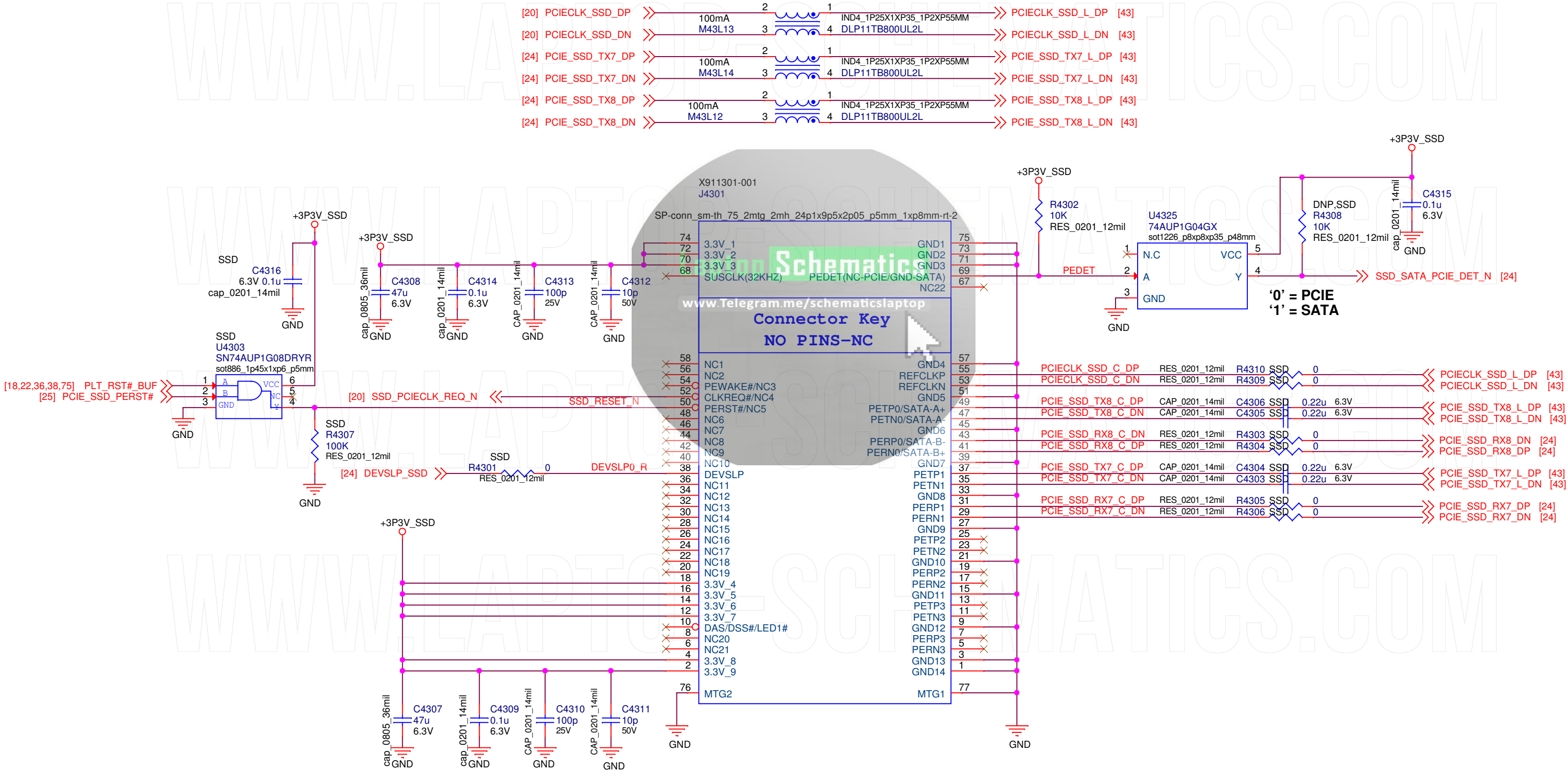


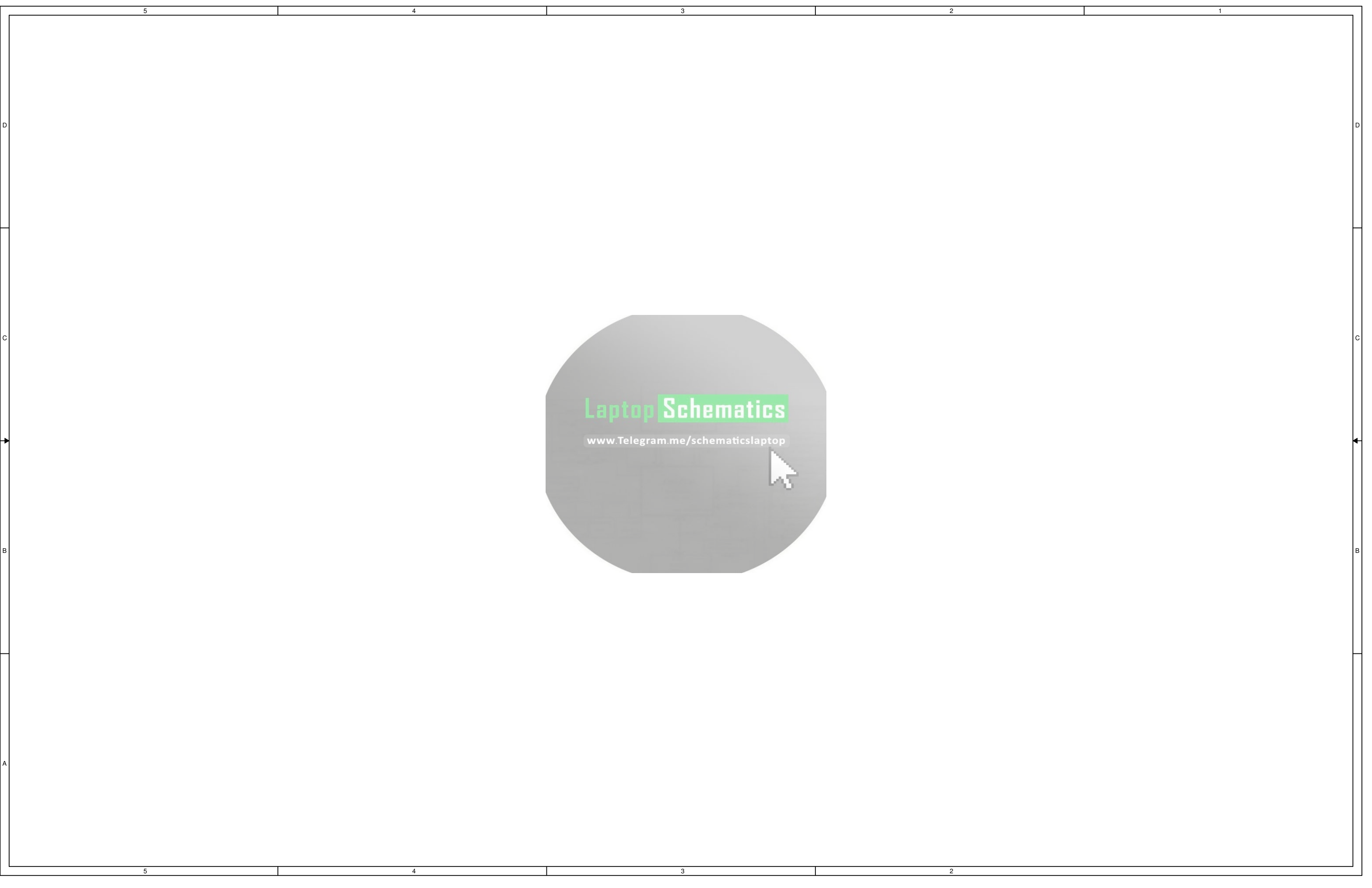


Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen2/SATA	PCI Express* Gen3/SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.

3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.

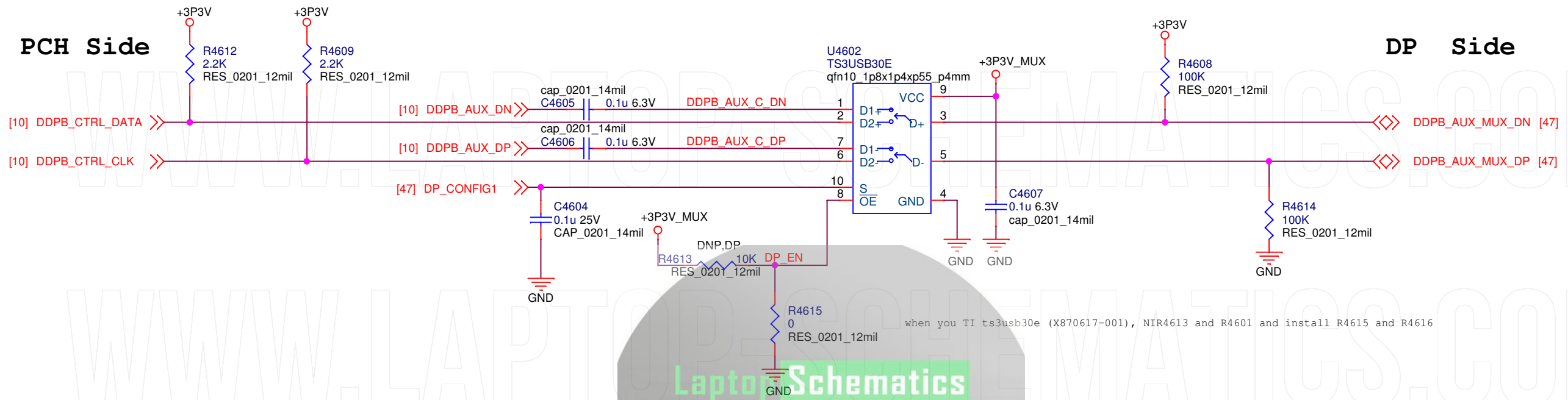




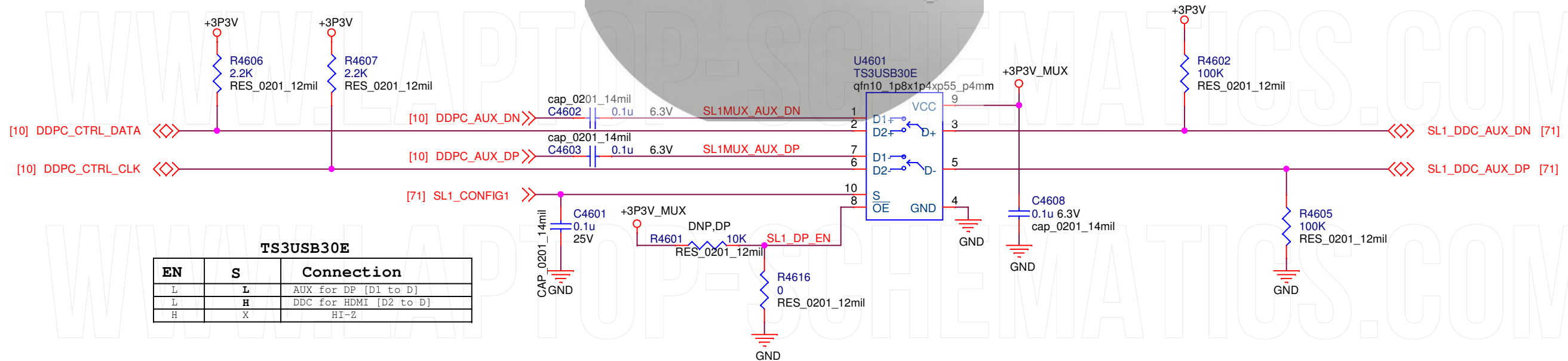
Laptop Schematics

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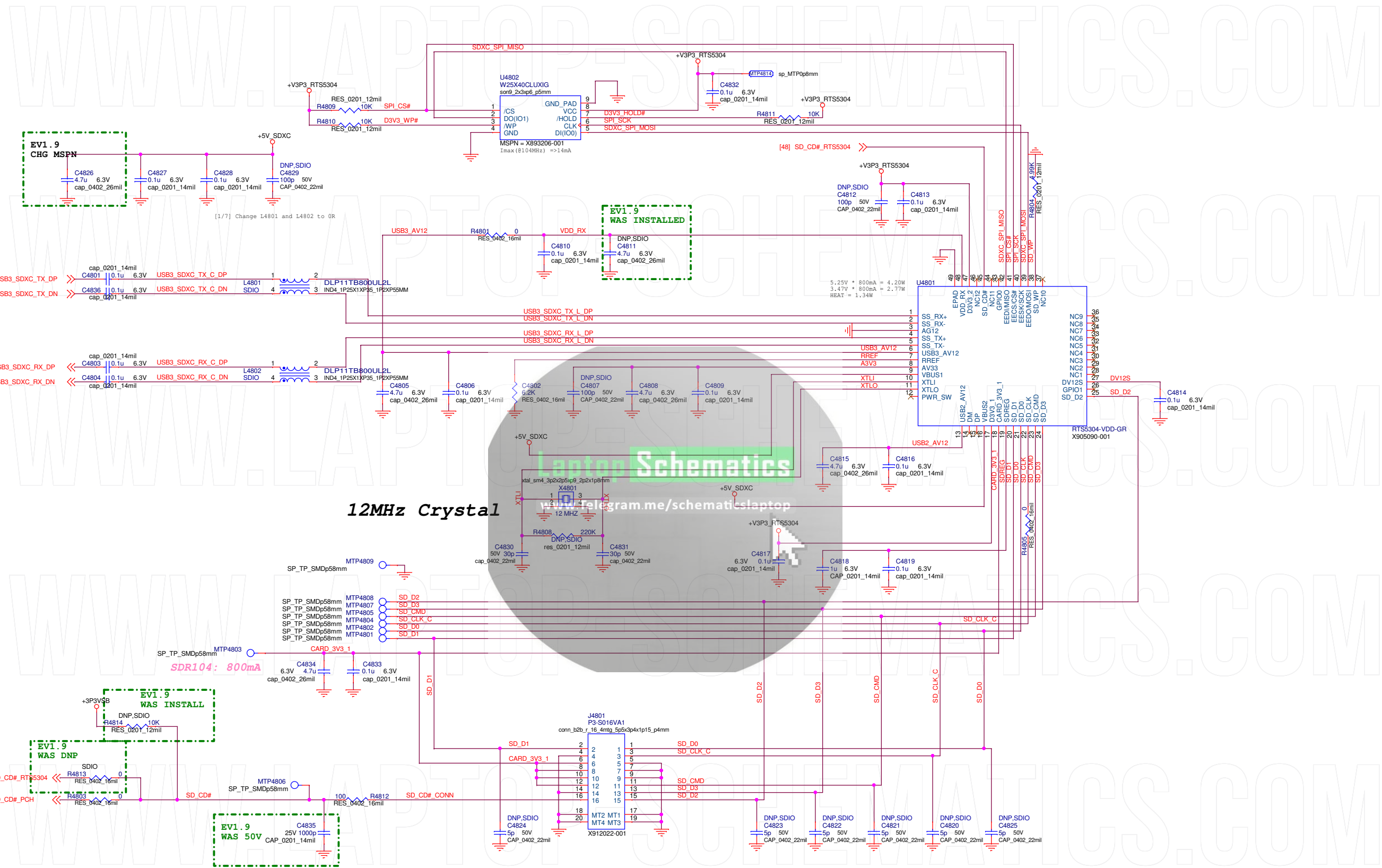
mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control

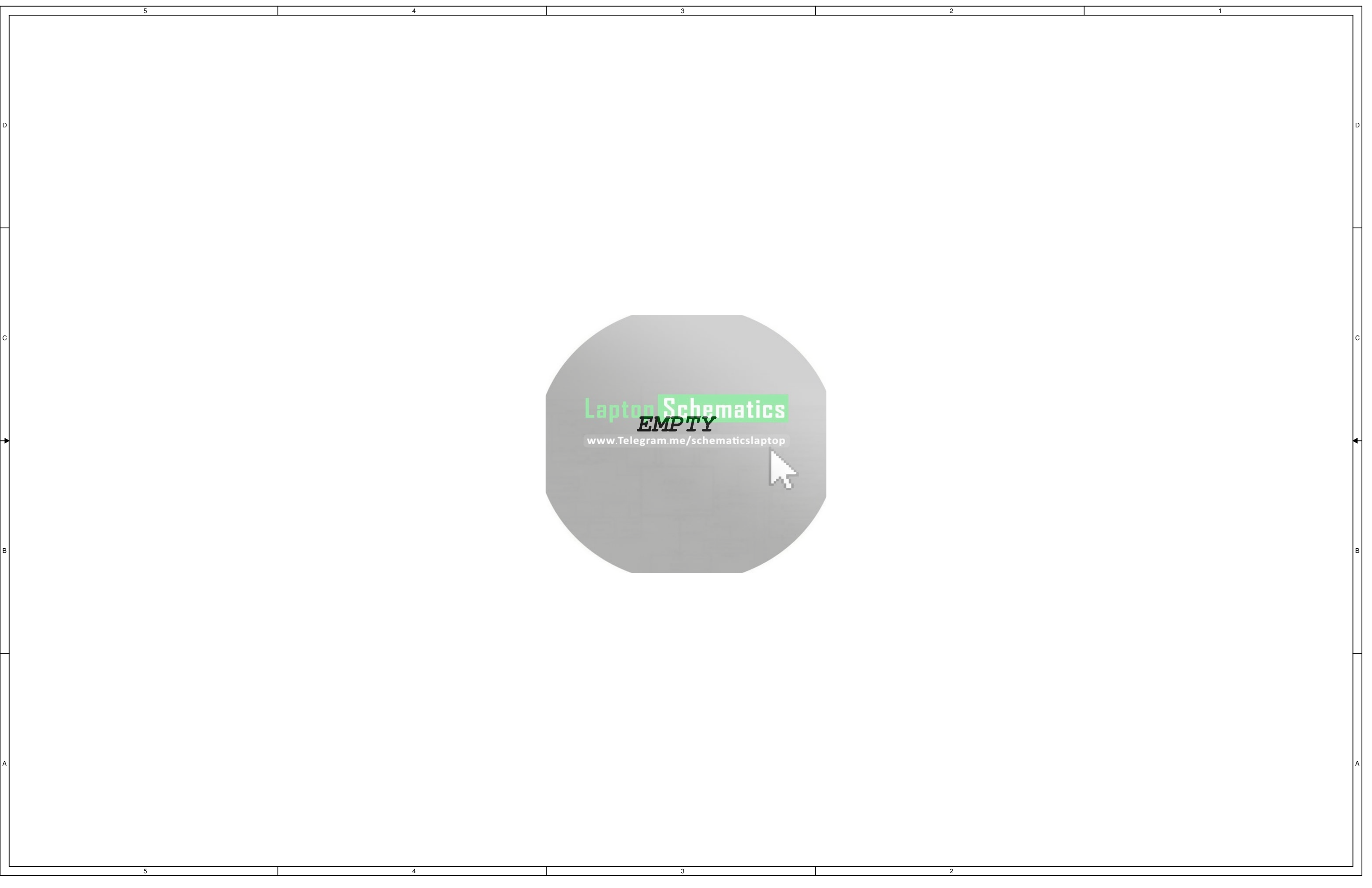












5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

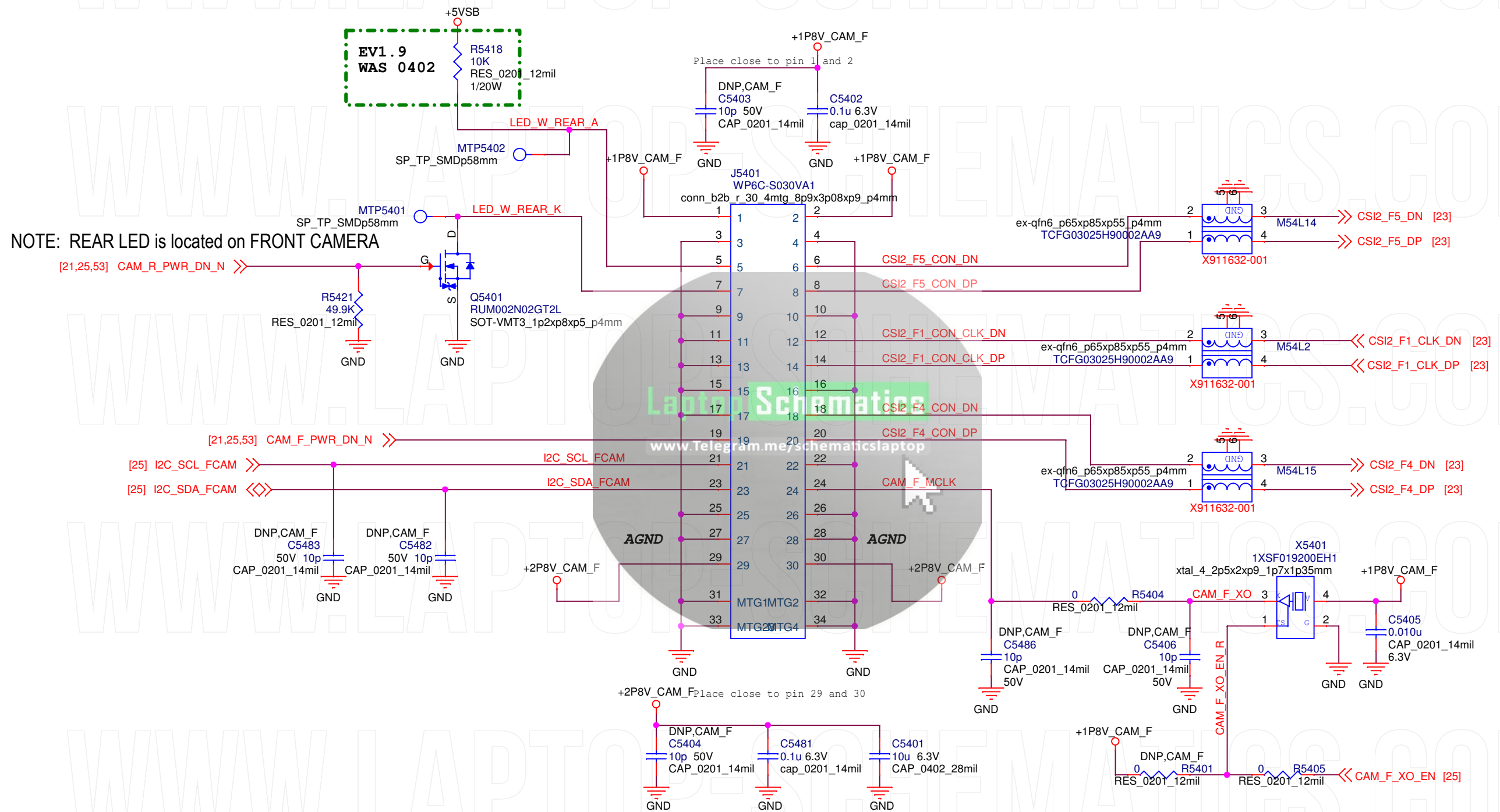
2

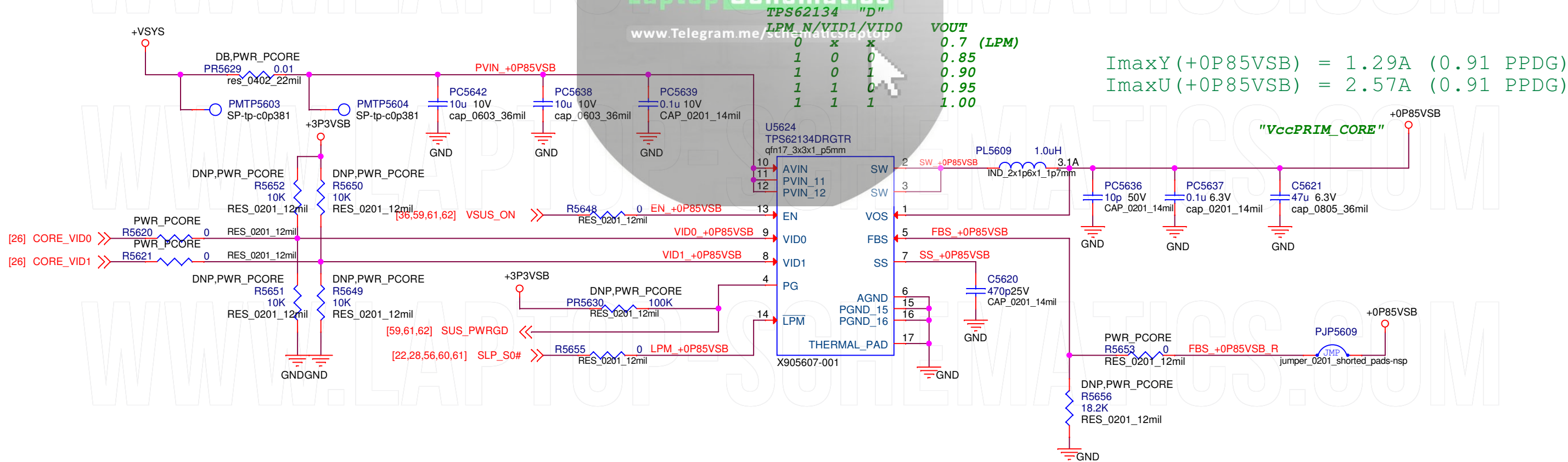
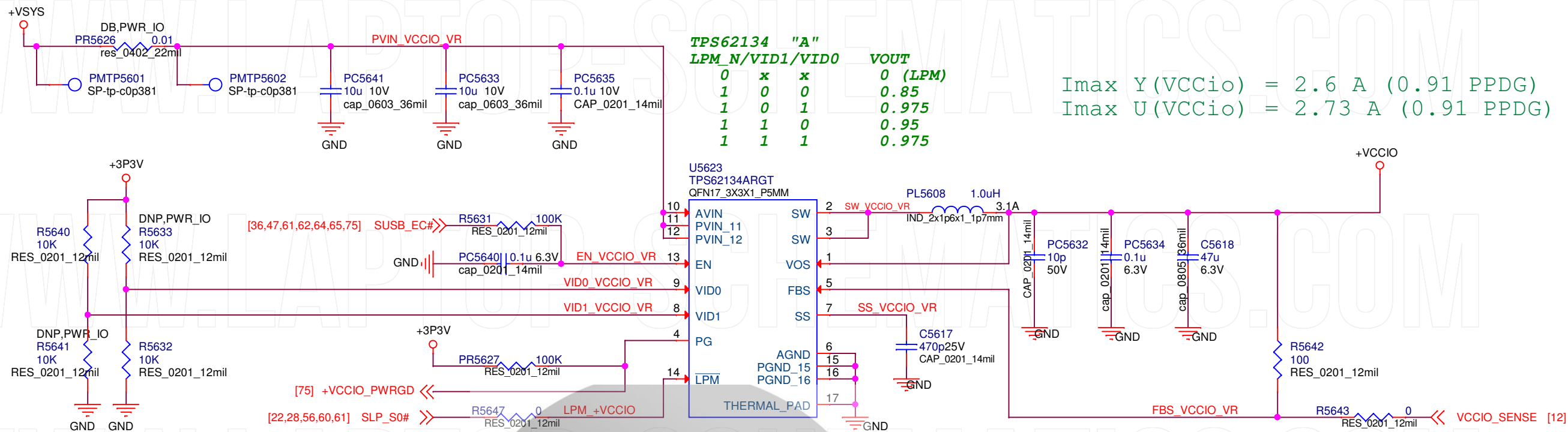
Laptop Schematics

EMPTY

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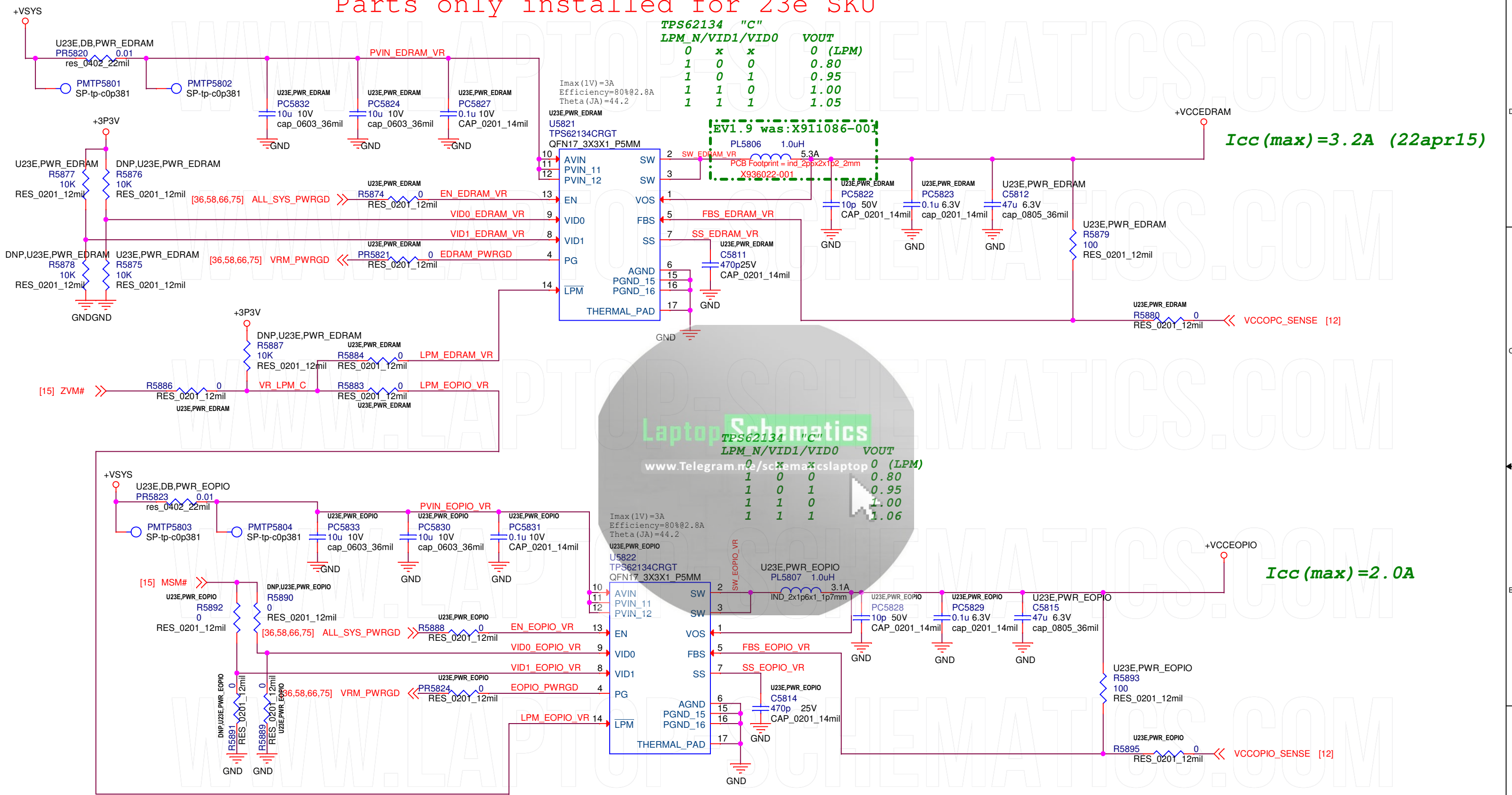




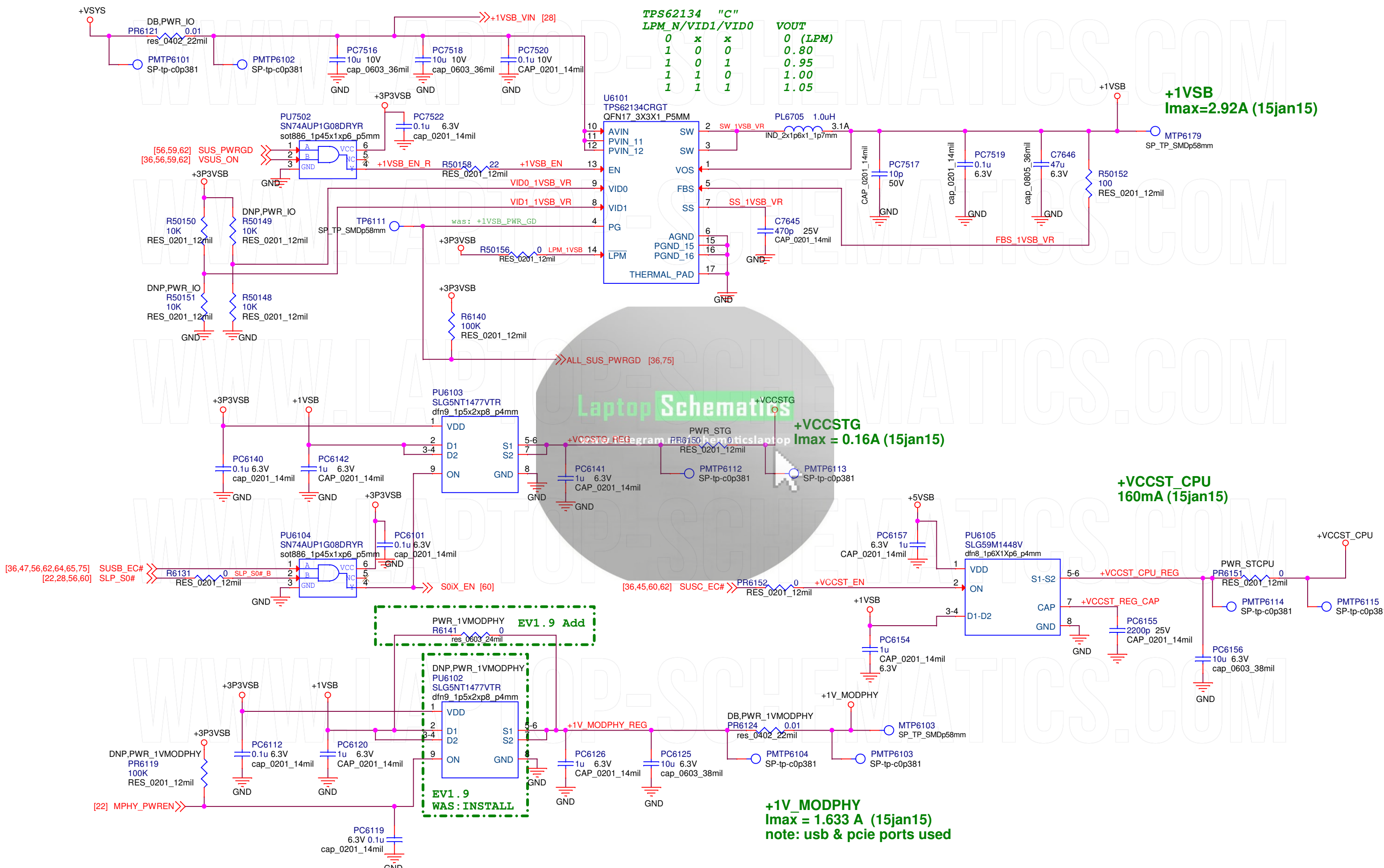




Parts only installed for 23e SKU

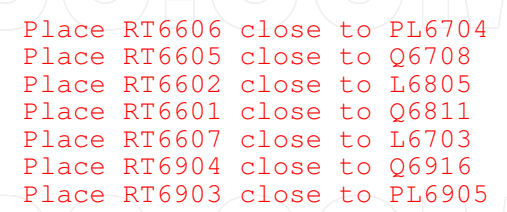






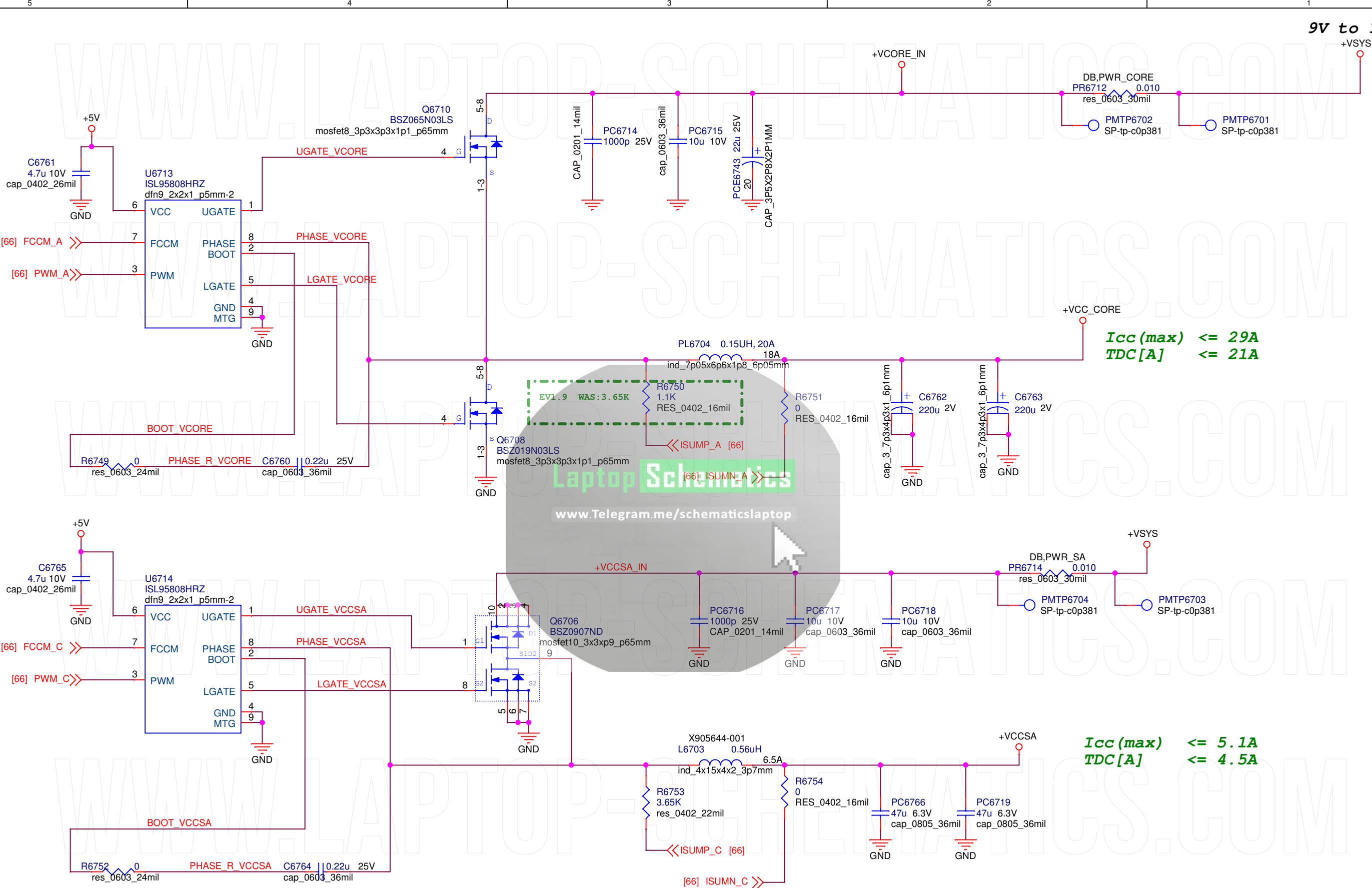


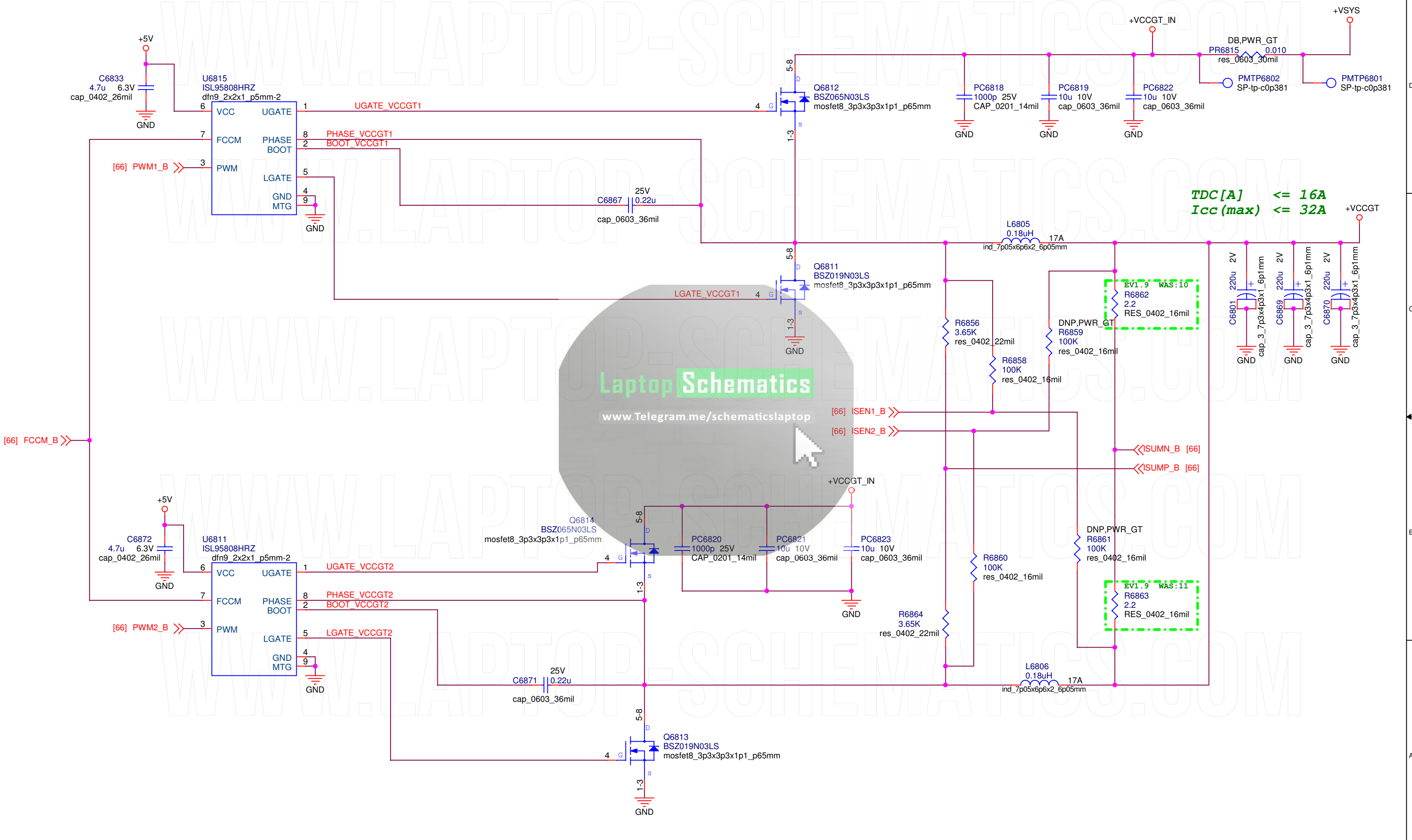




	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
Intel SPEC		
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	57A/32A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
ICCMAX/TDC of VCCGTx	N/A	7A/4A
DC_LL of Vcore	2.35 mohm	2.1 mohm
DC_LL of VCCGT	3.1 mohm	2 mohm
DC_LL of VCCSA	10.3 mohm	10.3 mohm
DC_LL of VCCGTx	N/A	6.9 mohm
Change items		
Vcore	No need to changed	No need to changed
VCCGT	R6674 : 150kohm (ICCMAX) R6640 : 1.24kohm (60A OCP) R6644 : 3.09kohm (LL 3.1mohm)	R6674 : 165 kohm (ICCMAX) R6640 : 1.69kohm (80A OCP) R6644 : 2.68kohm(LL 2mohm)
VCCSA	No need to changed	No need to changed
VCCGTx	Disable U6916	Enable U6916

	U22	U23E
R6674	150K	165K
R6696	90.9K	88.7K
R6644	3.92K	3.09K
C6624	680pF	390pF
R6640	1.24K	1.69K
R6602	150K	121K
R6618	118K	100K

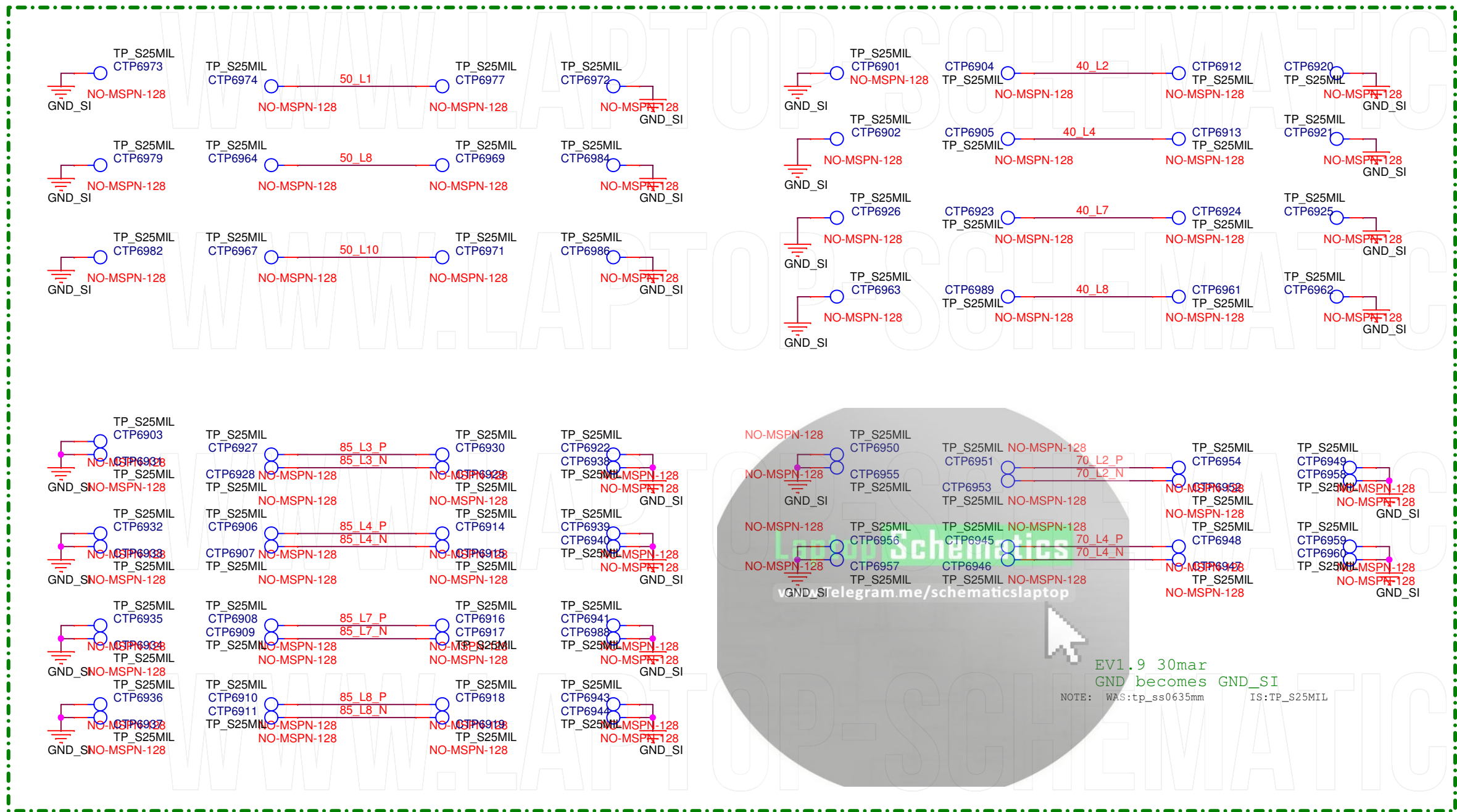




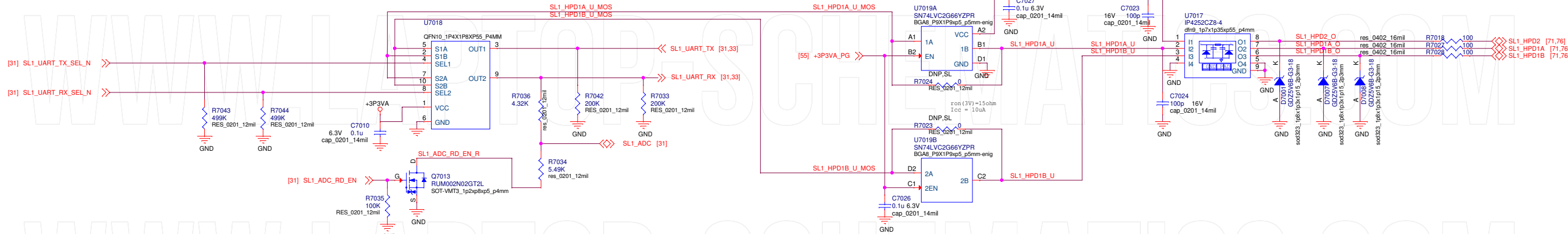
Laptop Schematics

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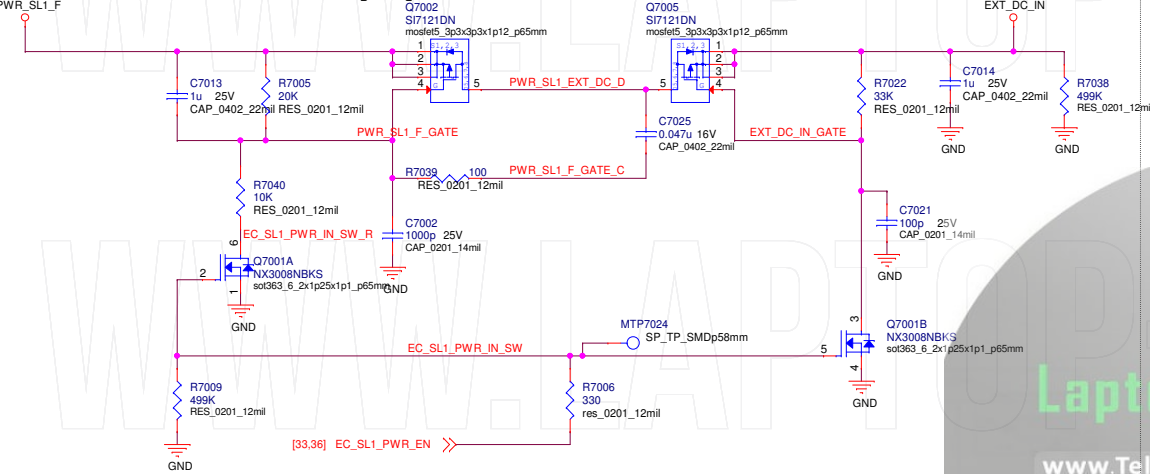
TDC[A] <= 16A
Icc(max) <= 32A



HPD FOR SL1 (ONE/TWO WIRE UART)



[In] SL1 6-12V PWR to EXT DC IN



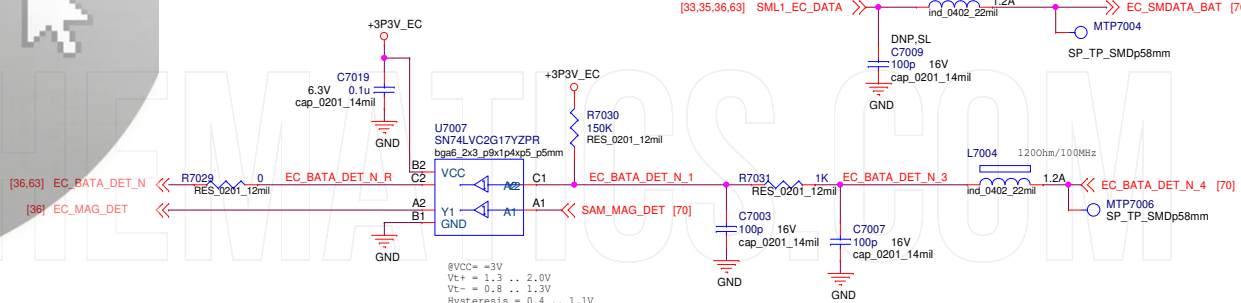
Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

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TPS3700 (Voltage Comparator)

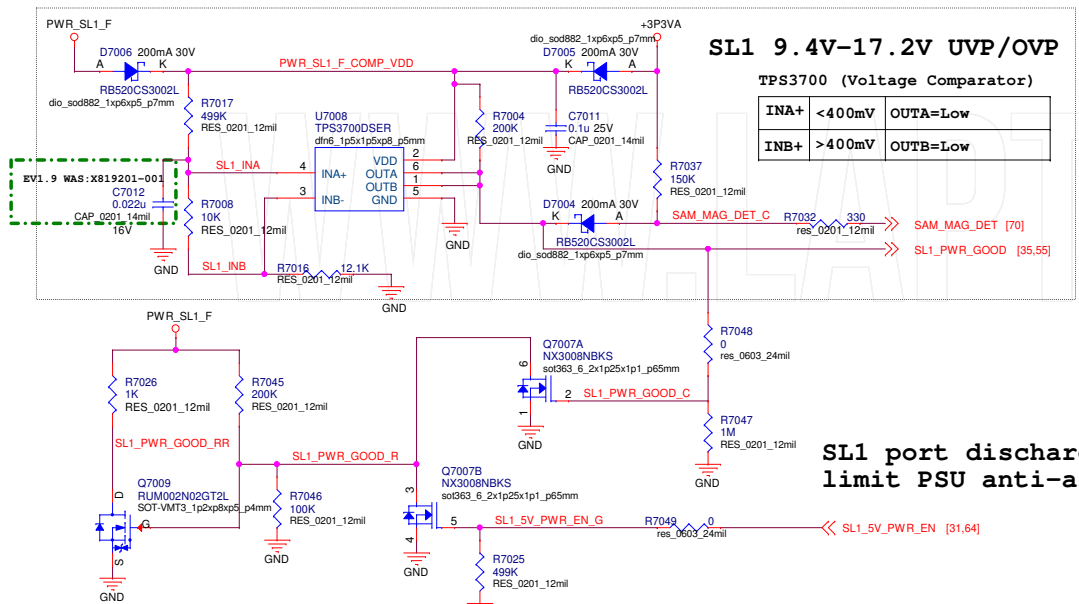
INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

CHG_ACDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES



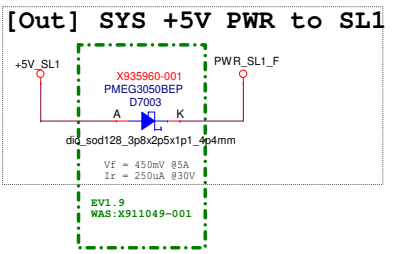
SL1 9.4V-17.2V UVP/OVP

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low



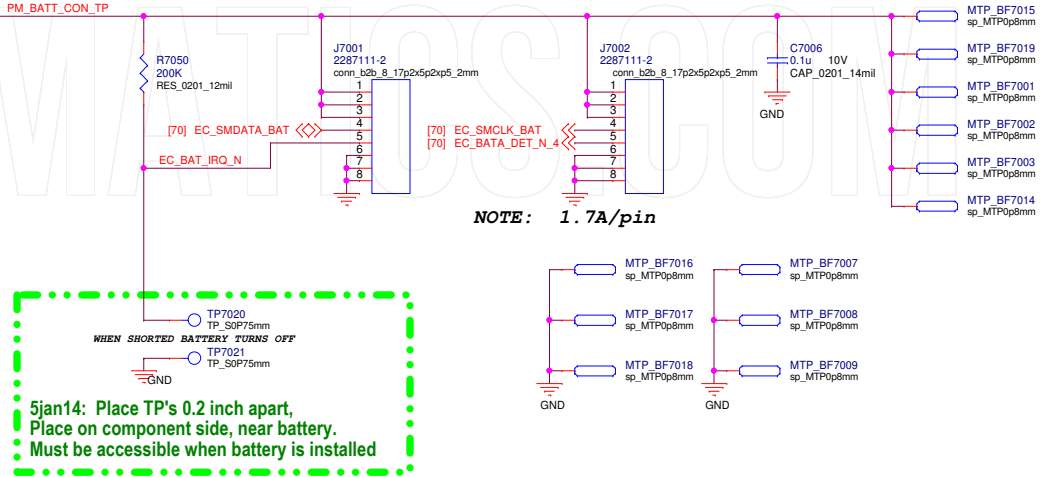
SL1 port discharger limit PSU anti-arc pulse voltage

$$Tablet2SL = 1.5/2A$$



40W Battery Connector

7-bit I2C Address = 0x??



5jan14: Place TP's 0.2 inch apart, Place on component side, near battery. Must be accessible when battery is installed

[31] SL1_3P3V_DIS

isolated ground on layer 2 to tie Cin GND, Cout GND, and controller PGND together. Then tie this isolated ground plane to main GND under the exposed pads.

+VCC_EDP_BKLT_IN
I_{max}=??A
TDC=??A

jks 15dec14:
EffCap (10u@28V) = 1.5uF
EffCap (4.7u@28V) = 0.8uF
Novatek: Cout = 4.7uF

Novatek 15dec14: I_{peak}(Vin=6V) = 1.144A

EV1.9
was: INSTALL

EV1.9
WAS NNT50273QG/A

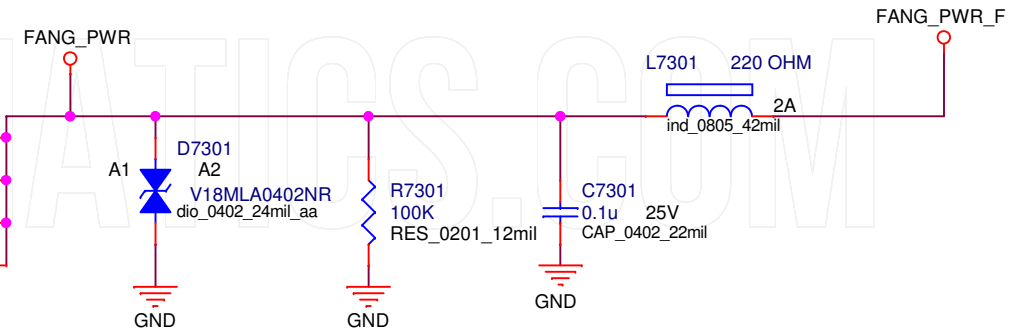
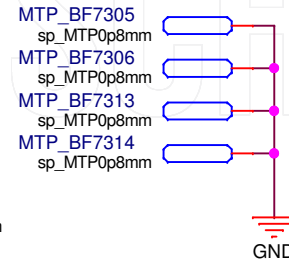
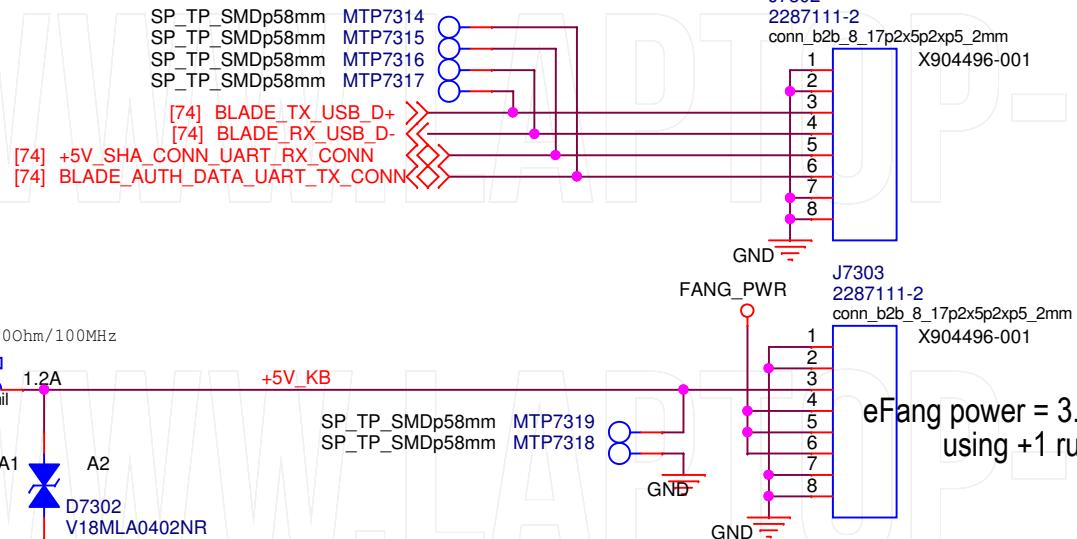
EV1.9 install

- MTP7202 SP_TP_SMDp58mm << BKLT_FB1 [57,72]
- MTP7203 SP_TP_SMDp58mm << BKLT_FB2 [57,72]
- MTP7206 SP_TP_SMDp58mm << BKLT_FB3 [57,72]
- MTP7210 SP_TP_SMDp58mm << BKLT_FB4 [57,72]
- MTP7204 SP_TP_SMDp58mm << BKLT_FB5 [57,72]
- MTP7205 SP_TP_SMDp58mm << BKLT_FB6 [57,72]
- MTP7207 SP_TP_SMDp58mm << BKLT_FB7 [57,72]
- MTP7208 SP_TP_SMDp58mm << BKLT_FB8 [57,72]

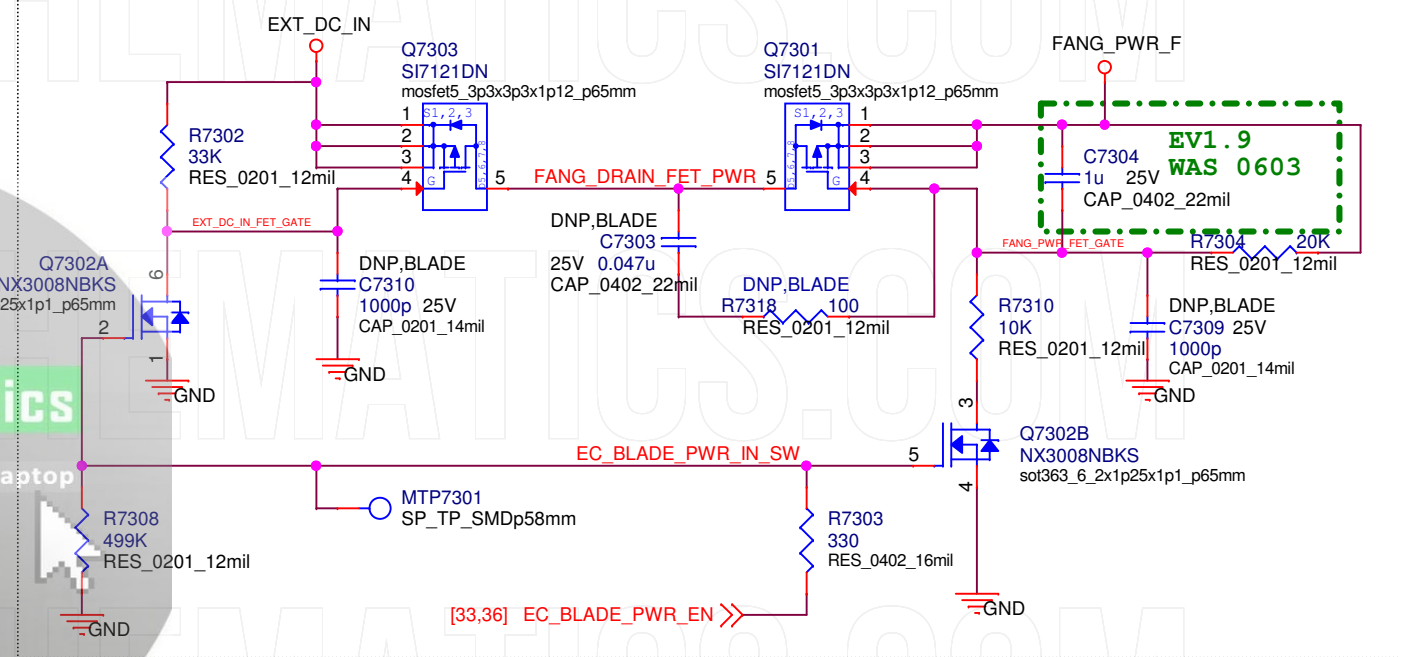
- | | | | | | |
|----|------------|----------------|-------|---|---------------------|
| 7 | BKLT_FB8_R | RES 0201 12mil | R7218 | 0 | << BKLT_FB8 [57,72] |
| 8 | BKLT_FB7_R | RES 0201 12mil | R7219 | 0 | << BKLT_FB7 [57,72] |
| 9 | BKLT_FB6_R | RES 0201 12mil | R7220 | 0 | << BKLT_FB6 [57,72] |
| 10 | BKLT_FB5_R | RES 0201 12mil | R7221 | 0 | << BKLT_FB5 [57,72] |
| 12 | BKLT_FB4_R | RES 0201 12mil | R7222 | 0 | << BKLT_FB4 [57,72] |
| 13 | BKLT_FB3_R | RES 0201 12mil | R7223 | 0 | << BKLT_FB3 [57,72] |
| 14 | BKLT_FB2_R | RES 0201 12mil | R7224 | 0 | << BKLT_FB2 [57,72] |
| 15 | BKLT_FB8_1 | RES 0201 12mil | R7225 | 0 | << BKLT_FB1 [57,72] |

+5V_KB_CONN
Imax = 0.5A

BLADE Connector

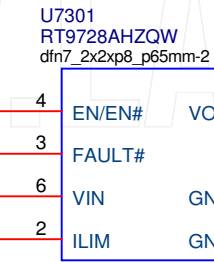


[In] BLADE 6-12V PWR to EXT DC IN Imax=4.5A

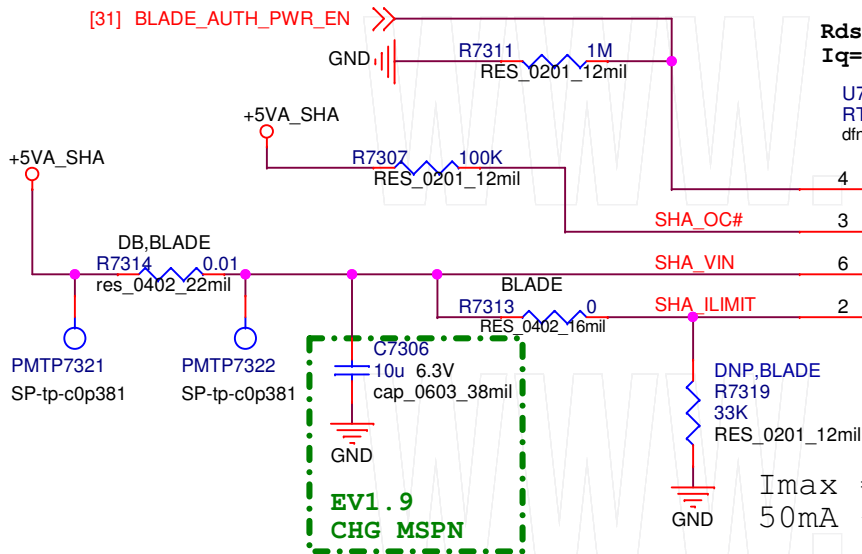


+5V_SHA_CONN
Imax=75mA

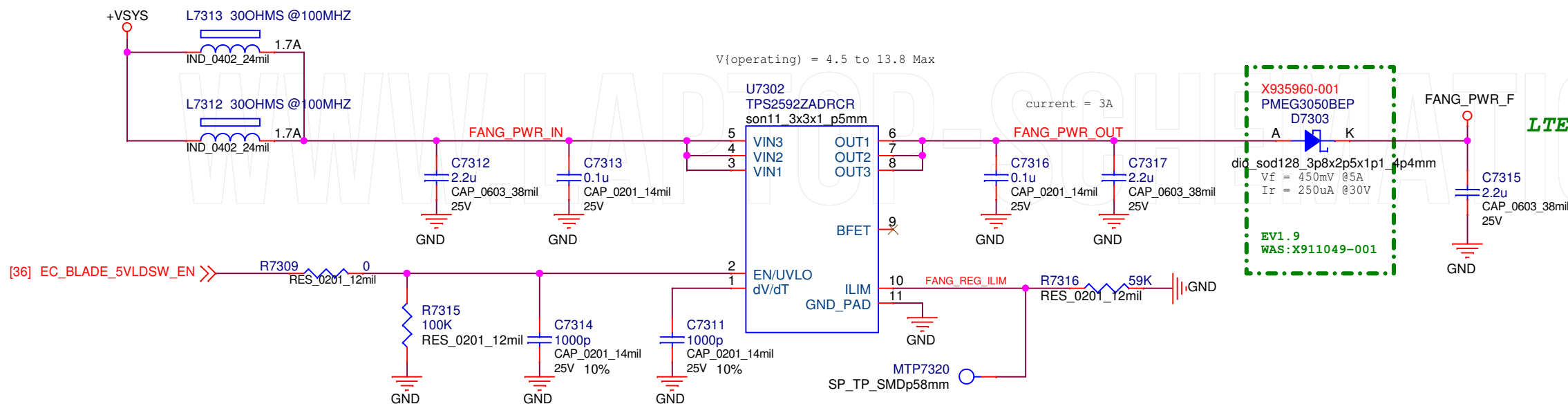
Rds(on) = 120mOhm (typ)
Iq = 170uA



Imax = 1.4A
50mA <= ILIM (connected to VIN) <= 100mA



V(operating) = 4.5 to 13.8 Max



LTE eFANG PWR = 2.10A(min)
2.47A(nom)
2.84A(max)

